Divide by n with the 7490—and do it without external parts. Merely wire between pins. All circuits except one also provide a BCD output.

Probably no other IC counter is as popular or as widely available as the 7490 decade counter. As ICs go, it is ancient it was introduced at least seven years ago. Although it was originally designed to provide only a divide by two, by five or by 10, or a BCD count-of-10 sequence, the 7490 can also be connected to divide by an integer from two to 10—and without external components. All that is needed is correct wiring between pins (see accompanying table).

From the logic designer's point of view, to pick apart the details of the schematic of the
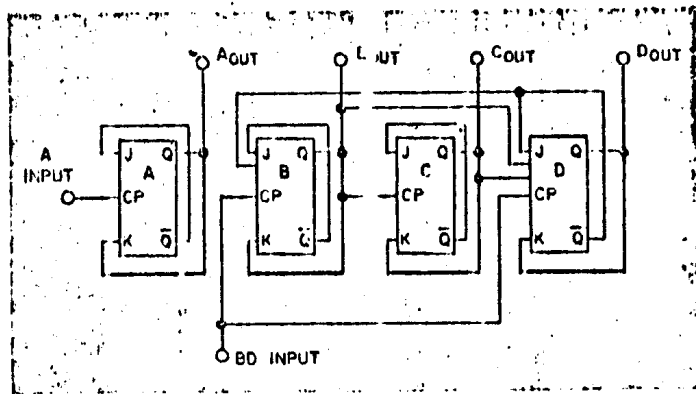
Dr. Roger Camp, Iowa State University, Ames, Iowa 50010.

1. A simplified block diagram supplies the details of the 7490's J-K inputs that are important to the design of the divide-by-n circuits.
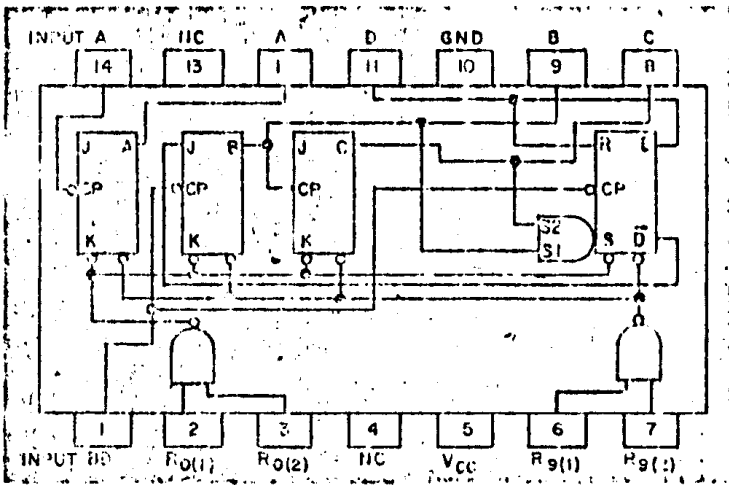
RESET/COUNT

RESET INPUTS				OUTPUT			
$R_{0(1)}$	$R_{0(2)}$	$R_{9(1)}$	$R_{9(2)}$	D	C	B	A
1	1	0	X	0	0	0	0
1	1	X	0	0	0	0	0
X	X	1	1	1	0	0	1
X	0	X	0	COUNT			
0	X	0	X	COUNT			
0	X	X	0	COUNT			
X	0	0	X	COUNT			

2. The reset/count truth table shows the reset input conditions for setting the 7490 to the ZERO, binary-9 or count condition.

counter serves little purpose. Every manufacturers' specification sheet provides an identical schematic drawing. Briefly stated, the 7490 is made up of four J-K master-slave flip-flops (Fig. 1). These flip-flops are separated into two independent circuits, with the A flip-flop separate from the B, C, D combination. The A circuit is a divide-by-two and the B, C, D a divide-by-five. In addition there are two dual-input NAND gates to provide nonclocked direct setting to the all-ZERO or to the binary-9 state.

Of the four flip-flops, only on the A and C flip-flops do the true and complementary outputs alone connect back to their K and J steering inputs, respectively. Thus every falling signal edge to the CP trigger inputs of flip-flops A or C causes them to complement. But the B and D flip-flops have additional AND inputs to their J steering points that modify the behavior of these flip-flops: They toggle only on specific falling CP signal edges, to make the B, C and D flip-flops work as a divide-by-five circuit.

For simplicity, the reset-to-ZERO and reset-to-binary-9 gates have been omitted from the block diagram of Fig. 1. These gates are conventional TTL, NAND gates. If both inputs in either gate are high, the low output forces both the master and slave flip-flops of the respective circuits to the desired ZERO or binary-9 states (Fig. 2).

Unfortunately, the block diagrams provided by manufacturers (Fig. 3) leave out important details of the 7490 circuitry. This obscures some possibilities for unconventional counter designs. Note that the J-K steering inputs for the flip-flops are not shown in full detail and that the details for D are, at best, unclear.

Division by integers two to ten

The conventional BCD decade connection is shown in Fig. 4a. If a symmetrical square-wave output is required in a divide-by-10 configuration, use Fig. 4b. However, Fig. 4b does not provide a BCD output code. Since it uses the counter's divide-by-five section followed by the divide-by-two, this arrangement results in a modulo-5 and modulo-2 residual code.

The concept behind dividing by an integer between 2 and 10 is as follows: One or two output variables can be returned to either the reset-to-ZERO or reset-to-NINE inputs. This allows the count to continue from the ZERO or binary-9 state until the reset state is again reached. Some of the possible connections for the 7490 in a divide-by-n counting mode are given in the table. The average logic designer can readily verify for himself that each of the configurations works as described. ■■

3. Manufacturers' block diagrams provide pin arrangements and the reset-circuit internal wiring, but leave out the important J-K input details.
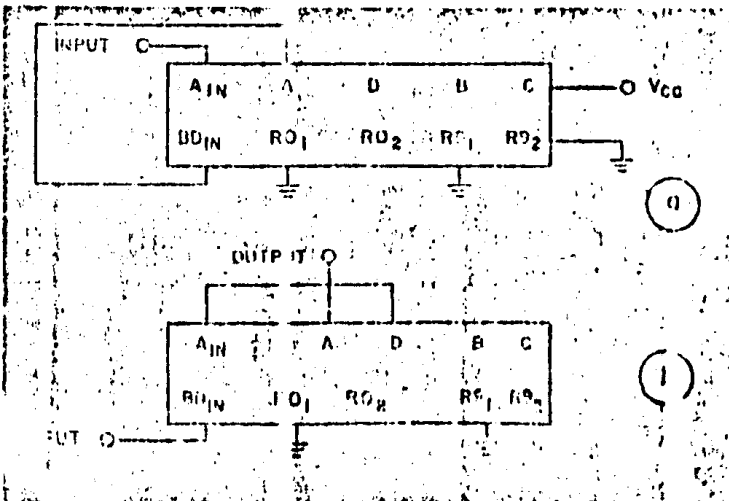
4. The counter configurations provided on spec sheets are only (a) a conventional BCD counter hook-up and (b) a symmetrical-wave output divide-by-ten.

Hookups for 7490 divide-by-n counting

n	CONFIGURATION	REMARKS
2		+ 5 SECTION UNUSED
3		BCD COUNT OBTAINED ON FLIP-FLOPS A AND B
4		BCD COUNT OBTAINED ON FLIP-FLOPS A AND B
5		BCD COUNT OBTAINED ON FLIP-FLOPS A, B AND C
		A IS UNUSED, BCD COUNT OBTAINED ON FLIP-FLIPS B, C AND D
6		BCD COUNT OBTAINED ON FLIP-FLOPS A, B AND C
7		RESET-TO-NINE USED. BCD COUNT NOT AVAILABLE
8		BCD COUNT OBTAINED ON FLIP-FLOPS A, B, C AND D
9		CD COUNT OBTAINED ON LIP-FLOPS A, B, C AND D
10		CIRCUIT OBTAINED ON FLIP-FLOPS A, B, C AND D