Errata

Title & Document Type: 3586A/B/C Selective Level Meter Service Manual - Volume 2

Manual Part Number: 03586-90002V2

Revision Date: May 1983

HP References in this Manual

This manual may contain references to HP or Hewlett-Packard. Please note that Hewlett-Packard's former test and measurement, semiconductor products and chemical analysis businesses are now part of Agilent Technologies. We have made no changes to this manual copy. The HP XXXX referred to in this document is now the Agilent XXXX. For example, model number HP8648A is now model number Agilent 8648A.

About this Manual

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Search for the model number of this product, and the resulting product page will guide you to any available information. Our service centers may be able to perform calibration if no repair parts are needed, but no other support from Agilent is available.

Agilent Technologies

SERVICE MANUAL

SELECTIVE LEVEL METER

3586A/B/C

VOLUME II

Service

HEWLETT PACKARD

HEWLETT PACKARD

SERVICE MANUAL

MODEL 3586A/B/C SELECTIVE LEVEL METER

(Including Options 001, 002, 003, and 004)

VOLUME II

IMPORTANT NOTICE

This manual applies to all instruments. Earlier versions of the 3586A/B/C, however, may differ in design and appearance from the instruments this revision documents directly. Changes that have been made to the instrument and which affect the instrument's documentation are identified by the delta (Δ) symbol. The "numbered" Δ refers the reader to the corresponding numbered Δ in the backdating section (Section VII) in Volume I of the 3586A/B/C Service Manual.

WARNING

To prevent potential fire or shock hazard, do not expose equipment to rain or moisture.

This service manual contains no operating information. For Sections I to III (Operation), see the 3586A/B/C Operating Manual (Part No. 03586-90012, Microfiche Part No. 03586-90062).

Manual Part No. 03586-90002
Microfiche Part No. 03586-90052

P.O. Box 301, Loveland, Colorado, 80537 U.S.A.

Printed: May, 1983

3586A/B/C Service Manual Volume II
Quick Reference Guide

SECTION VIII
SERVICE

NOTE

Do not remove any of the covers of the 3586A/B/C until you have read the information contained in Paragraphs 8-1 through 8-7.

8-1. INTRODUCTION.

8-2. This volume of the Service Manual contains information relative to the maintenance and service of the 3586A/B/C Selective Level Meter. The information presented in this manual is assembled into four major segments: Turn-on Initialization and Milking the Front Panel, Troubleshooting, Detailed Functional (circuit) Description, and Service Groups. Where references are made throughout the manual to a performance test, adjustment procedure, the parts list, or backdating section, refer to Volume I: 3586 Performance Tests, Adjustments, Parts, and Backdating. In order to obtain a minimum of instrument down time and to provide for the greatest amount of troubleshooting efficiency and safety, it is recommended that Safety Considerations (paragraph 8-5), Use Of The Service Manual (paragraph 8-8), and Service Volume Organization (paragraph 8-11) be read before initiating any troubleshooting procedures.

8-3. SPECIFICATIONS.

8-4. Table 8-1 is a complete list of the Model 3586A/B/C critical specifications that are controlled by tolerances. Specifications listed in this manual supersede all previous specifications for the Model 3586A/B/C.

Table 8-1. 3586A/B/C Performance Specifications.

FREQUENCY

Frequency Range And Signal Inputs:

Signal Input	3586A	3586B	3586C
75Ω/50Ω/10kΩ Unbalanced	200 Hz to 32.5 MHz		
124Ω Balanced		4 kHz to 10 MHz	
135Ω Balanced		4 kHz to 1 MHz	
150Ω Balanced	4 kHz to 1 MHz		
600Ω/Bridged	100 Hz to 108 kHz		

The 50Ω, 75Ω, 10 kΩ, 124Ω, 135Ω, 150Ω and 600Ω inputs are usable over wider frequency ranges than specified.

Frequency Resolution:
0.1Hz

Center Frequency Accuracy:
$\pm 1 \times 10^{-5}$/year, ($\pm 2 \times 10^{-7}$)/year with option 004

Counter Accuracy:
±1.0Hz in addition to center frequency accuracy for signals within the 60dB bandwidth of the IF filter chosen or greater than −100dBm, (largest signal measured).

Frequency Display:
9 digit LED

Table 8-1. 3586A/B/C Performance Specifications (Cont'd).

SELECTIVITY

3dB Bandwidth, ±10%:

3586A (CCITT)		3586B (No. American)		3586C (General)
Standard	**Option 003**	**Standard**	**Option003**	**Standard**
20Hz	20Hz	20Hz	20Hz	20Hz
400Hz	400Hz	400Hz	400Hz	400Hz
1740Hz*	3100Hz	2000Hz**	3100Hz	3100Hz
-	Psophemotric Noise Weighting	-	C-Message Noise Weighting	

* Psophometric *Equivalent Noise Weighting Filter.*
** C-Message *Equivalent Noise Weighting Filter.*

Adjacent Channel Rejection:

75dB minimum at ±2850Hz, 3100Hz BW; ±2500Hz, 2000Hz BW; ±2350Hz, 1740Hz BW.

Carrier Rejection:

Bandwidth	60db Points (Max)
3100Hz	±1850Hz
2000Hz	±1500Hz
1740Hz	±1350Hz

400Hz Bandwidth 60dB Rejection:

±1100Hz

20Hz Bandwidth Rejection:

30dB, ±45Hz; 60dB, ±90Hz

Passband Flatness:

Bandwidth	Flatness Range	Flatness
3100Hz	±1000Hz	±0.3dB
2000Hz	± 650Hz	±0.3dB
1740Hz	± 550Hz	±0.3dB
400Hz	± 50Hz	±0.3dB
20Hz	± 3Hz	±0.3dB

AMPLITUDE

Measurement Range:

+25 to −120dBm

Note that the **specified** measurement range is +20 to −100 dBm.

Amplitude Resolution:

.01dB

Level Accuracy:

10dB auto range, low distortion mode, after calibration (For the 3586C; 75Ω, 50Ω, and 600Ω, inputs; below −80dBm; these specifications apply only when using the 20Hz and 400Hz bandwidths).

75Ω/50Ω Input (3586A/B/C)

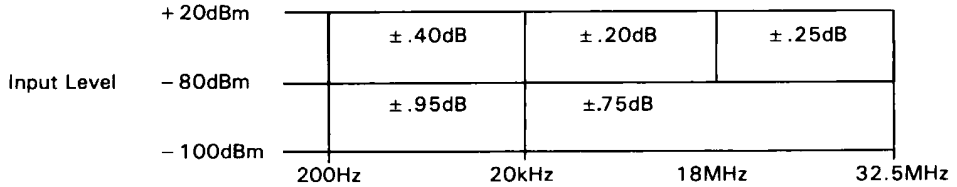
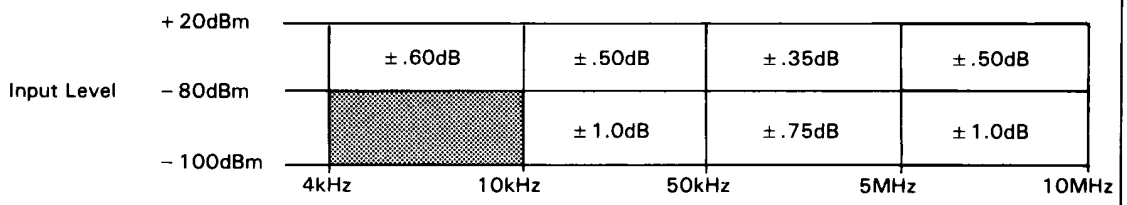
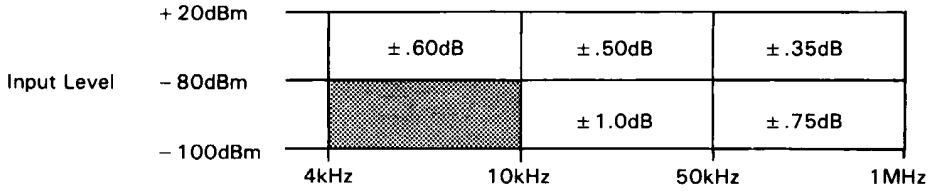


Table 8-1. 3586A/B/C Performance Specifications (Cont'd).

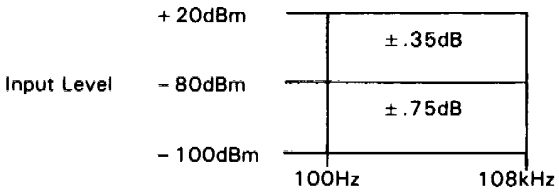
124Ω Input (3586B)



150Ω Input (3586A) or 135Ω Input (3586B)



600Ω Input (3586A/B/C)



Level Accuracy:

100dB Range (after calibration); add correction to 10dB auto range accuracy for dB below full scale. (Not required when in 10dB autorange.)

dB Below Full Scale	Accuracy Correction
0 to -20dB	± .25dB
-20 to -40dB	± .50dB
-40 to -80dB	±2.0 dB

DYNAMIC RANGE

Spurious Responses:

Image Rejection (100-132MHz):
-80dBc

IF Rejection:

15625Hz, -80dBc; 50MHz, -60dBc

Non-Harmonic Spurious Signals:

>1600Hz offset; -80dBc
300Hz to 1600Hz offset; -75dBc

Residual Spurious Signals:

≥350Hz, -115dBm (-110dBm for a 3586C)
<350Hz, -100dBm (-95dBm for a 3586C)

Table 8-1. 3586A/B/C Performance Specifications (Cont'd).

Distortion:

Harmonic Distortion:

70dB below full scale (−75dB for the 3586C), >4kHz on 75Ω and 600Ω inputs, Low Distortion Mode.

Intermodulation Distortion:

Two Tone 2nd and 3rd order, in band;
Separation 7kHz to 1MHz: either tone ≥10MHz, 70dB below full scale
Separation 7kHz to 1MHz: either tone <10MHz, 75dB below full scale (78dB for the 3586C)

Wideband Power Accuracy:

After calibration, 100dB auto range, averaging on, −45 to +20dBm;

±2.0dB	±1.0dB	±2.0dB
200Hz	20KHz	10MHz 32.5MHz

Noise Floor (Full Scale Setting −35 to −120dBm, AVE On Low Distortion Mode):

Frequency	Input	Bandwidth	Noise Level
100kHz to 32.5MHz	75Ω	1740Hz,2000Hz, or 3100Hz	−116dBm (−114dBm for a 3586C)
		400Hz or 20Hz	−120dBm
2kHz to 100kHz	75Ω,600Ω	All	−105dBm
100kHz to 10MHz	124Ω	1740Hz,2000Hz, or 3100Hz	−116dBm
		400Hz or 20Hz	−120dBm
100kHz to 1MHz	135Ω,150Ω	1740Hz,2000Hz, or 3100Hz	−116dBm
		400Hz or 20Hz	−120dBm
10kHz to 100kHz	124Ω,135Ω,150Ω	All	−105dBm

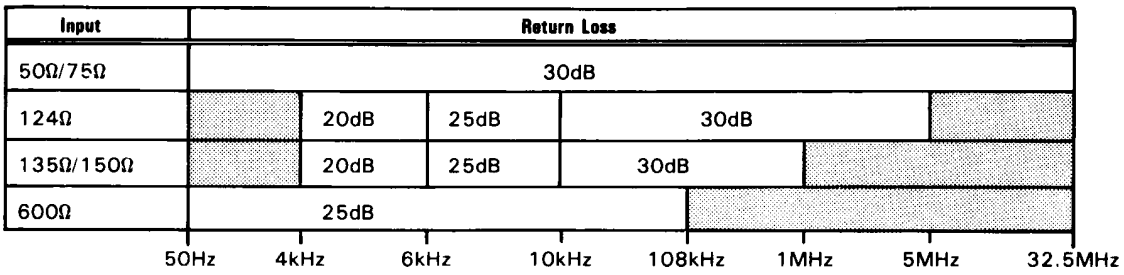
The noise floor for full scale settings of −30 to +25dBm will be 80dB below full scale for >100kHz, or 60dB below full scale for <100kHz. For the 3586C, the noise floor for full scale settings of −30 to +25dBm will be 75dB below full scale for >100kHz, or 55dB below full scale for <100kHz. These specifications do not apply to the 3586C's 50Ω input.

SIGNAL INPUTS

Model	Impedance	Frequency	Mating Connector
3586A	75 ohms unbalanced	200Hz to 32.5MHz	BNC
	150 ohms balanced	4kHz to 1MHz	Siemens 3-prong 9 Rel-6AC
	600 ohms balanced	100Hz to 108kHz	
3586B	75 ohms unbalanced	200Hz to 32.5MHz	WECO 439/440A (See Table 8-15 of Service Manual.)
	124 ohms balanced	4kHz to 10MHz	WECO 443A
	135 ohms balanced	4kHz to 1MHz	WECO 241A
	600 ohms balanced	100Hz to 108kHz	WECO 310
3586C	50/75 ohms unbalanced	200Hz to 32.5MHz	BNC
	600 ohms balanced	100Hz to 108kHz	Dual Banana Plug, 0.75 inch spacing

Table 8-1. 3586A/B/C Performance Specifications (Cont'd).

Return Loss:



Balance:

Input	Frequency	Balance
124Ω	10kHz to 10MHz	−36dB
135Ω or 150Ω	10kHz to 1MHz	−36dB
600Ω	50Hz to 108kHz	−40dB

DEMODULATED AUDIO OUTPUT

Demodulates an erect (USB) or inverted (LSB) SSB telephone channel, provides speaker or headphone output with volume control. Carrier is re-inserted at ±1850Hz to align channel filter precisely on a voice channel.

Output Level:

0dBm into 600Ω at full scale, adjustable

Output Connector:

Front Panel, mates with WECO 347 or 1/4" phone plug

TRACKING GENERATOR:

Level 0dBm at 10kHz, ±.5dB
Flatness 200Hz to 32.5MHz, ±.5dB

TRANSMISSION IMPAIRMENTS OPTION 003

Adds transmission impairment measurement capability to standard instrument. Measures phase jitter, noise with tone, single level impulse noise and weighted noise at voice channel and carrier frequencies. 3100Hz channel filter and C-message or psophometric weighted noise filter replaces the standard 2000Hz or 1740Hz equivalent noise filter.

Phase Jitter:

A phase jitter measurement can be made at any input signal frequency up to 32.5MHz that produces a 960-1060Hz tone in the demodulated output. Meets BSP 41009 and CCITT recommendation 0.91.

Demodulated Tone Frequency:

960 to 1060Hz

Input Signal Level:

≤30dB below full scale, −65dBm minimum

Frequency Response:

20 to 300Hz

Accuracy:

±(10% + .5° p-p)

Residual Phase Jitter:

≤.5° p-p (50kHz to 32.5MHz)

Table 8-1. 3586A/B/C Performance Specifications (Cont'd).

Weighted Noise Filters:

Psophometric weighting filter (3586A) complies with CCITT Recommendation P.53 and C-message weighting filter (3586B) complies with BSP 41009 response. When the noise weighting filter is enabled it is superimposed on the 3100Hz channel filter response.

Accuracy:

In addition to full scale accuracy, after calibration

800Hz (Psophometric, 3586A):

±0.5dB

1004Hz (C-Message, 3586B):

±0.5dB

Impulse Noise:

An impulse noise measurement can be made in a voice channel up to 32.5MHz. Meets BSP41009 or CCITT Recommendation 0.71. Used with 10db auto range only. The notch filter is automatically inserted, measurement can be made with or without a 1000Hz tone present.

Counting Rate of Impulse Noise:

3586A (CCITT):

125ms/count, ±5%

3586B (No. American):

143ms/count ±5%

Threshold Accuracy:

±1dB for a 1700Hz signal (with or without a 1000Hz tone applied 5dB above the threshold level), with a threshold level from 0 to 50db below full scale, or greater than −80dBm.

Notch Filter Rejection:

(Enabled during Noise with Tone and Impulse Noise measurements, Filter Response meets BSP41009.)

50dB minimum, 995 to 1025Hz.

GENERAL

Operating Environment

Temperature:
0° to 55°C

Relative Humidity:

95%. 0° to 40°C

Altitude:

≤15000 ft.

Storage Temperature:

−40°C to 75°C

Storage Altitude:

≤50,000 ft.

Table 8-1. 3586A/B/C Performance Specifications (Cont'd).

Power:
100/120/220/240V, +5%, −10% 48 to 66Hz, 150VA
Weight:
23Kg (50 lbs) net; 30Kg(65 lbs) shipping
Dimensions:
177mm high x 425.5mm wide x 466.7mm deep (7" high x 16.75" wide x 18.38" deep)

8-5. SAFETY CONSIDERATIONS.

8-6. Before applying power to the instrument or removing any of the covers, review the following warnings and cautions.

WARNING

These servicing instructions are for use by trained service personnel only. To avoid electrical shock, do not perform any servicing other than that contained in the operating instructions unless you are qualified to do so.

WARNING

Line voltage is present within the instrument even when the POWER switch is in STBY position. To prevent electrical shock, use care when working in the vicinity of the input power circuits.

WARNING

To protect operating personnel, the -hp- 3586A/B/C chassis and cabinet must be grounded. The -hp- 3586A/B/C is equipped with a three-wire power cord which, when plugged into an appropriate receptacle, grounds the instrument. The offset pin on the power plug is the ground connection. To preserve this protection feature, the power plug shall only be inserted in a three-terminal receptacle having a protective earth ground contact. The protective action must not be negated by the use of an extension cord or adapter that does not have the required earth ground connection. Grounding one conductor of a two-conductor outlet is not sufficient protection.

CAUTION

1. To prevent damage to the instrument power supply circuits, verify that the two line voltage select switches located on the instrument rear panel are selected to the correct line voltage (Figures 8-1 and 8-2) and the correct size line fuse is installed (Table 8-2).

2. The 3586A/B/C contains MOS devices which may become damaged as a result of static discharge.

3. To prevent equipment damage, do not remove circuit boards when the POWER switch is ON.

4. The regulated DC supply voltages are not individually fused. Accidentally shorting any of the supply buses together or to ground can cause major damage to the motherboard. In addition, the +15 vdc probe power is present at the front panel probe connector even in the STBY position of the POWER switch. (See Figure 8-A-1 for a pinout diagram of the probe power connector.)

8-7. Line Voltage Selection. Voltage selection switches on the rear panel are used to configure the instrument to operate on one of four input line voltage ranges. The range of input voltages for each configuration of the switches is illustrated in Figure 8-1. Set the switches to conform with the line voltage to be used with this instrument. The switch positions for each input voltage range are indicated on the rear panel and in Figure 8-2.

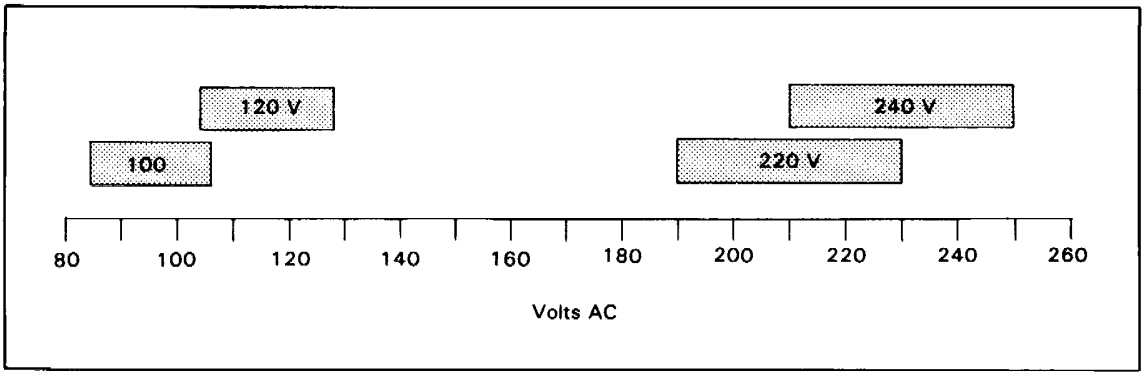


Figure 8-1. Input Range For Each Line Voltage Switch Selection.

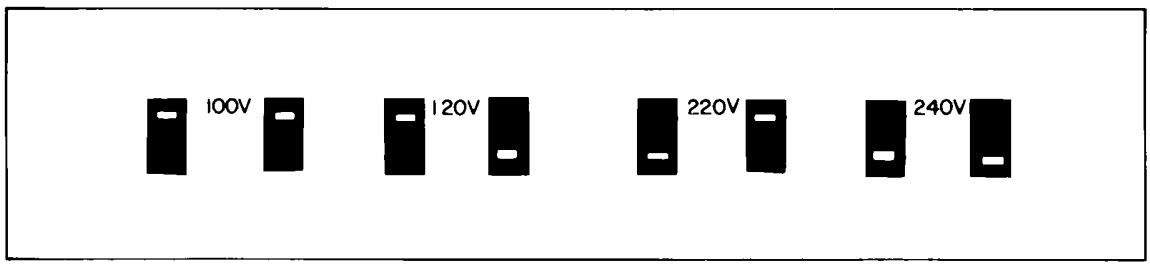


Figure 8-2. Switch Positions For Line Voltage Selection.

Table 8-2. Line Fuses.

Voltage Selector	Fuse Type	-hp- Part No.
100 V or 120 V	2 A, 250 V Fast BLO	2110-0002
220 V or 240 V	1A, 250V SLOW BLO	2110-0312

8-8. USE OF THE SERVICE MANUAL.

8-9. Service Information - How To Use It. After reading the section on the content and organization of this volume of the Service Manual, it may be apparent that a quick reference guide to the manual would be useful. Such a guide is provided as the last page of the section titled "Turn-On Initialization and Milking the Front Panel". This quick reference guide can be copied and placed elsewhere in the manual or it can be removed and used separately from the manual.

8-10. In trying to describe a method to follow for troubleshooting the 3586 there is a problem because of the differences in the number of units seen by technicians. The technician's familiarity with the instrument combined with his or her understanding of the symptoms of the malfunction often suggest various troubleshooting approaches. Outlined below are four troubleshooting approaches that the technician may wish to follow based on what is known or not known about the instrument. The technician may decide to use a combination of these approaches or develop an alternate method.

Method 1. If the technician is unfamiliar with the instrument or if the instrument malfunction is not clearly defined, the information under the heading "Turn-On Initialization and Milking the Front Panel" should be reviewed first. This section is a good starting point for aquainting oneself with the instrument and for establishing a troubleshooting path that will lead to the correct service group and eventual repair.

Method 2. The technician who has a good understanding of the 3586 may want to proceed directly to the Troubleshooting section of the manual. One may also wish to use the Major Signal Chart found in the troubleshooting section as well. The Turn-On Troubleshooting Flowchart and System Functional Block Diagram are useful tools in narrowing the problem down to a service group.

Method 3. The running of the Internal Self Tests found in the "Turn-On" section is a third approach which has been useful to technicians. These tests are a thorough front panel exercise which if used early in the troubleshooting process, can help identify the instrument malfunction and lead to the responsible service group.

Method 4. This method is very effective but requires taking the covers off of the instrument. The tracking output (Fo(0-32MHz)) on the back of the instrument normally has a 0dBm level at the frequency to which the front panel is tuned. It is assumed that a 75 ohm cable is used and that the signal is terminated into the 75 ohm input on the front panel. The functional block diagrams are all referenced to the following set of conditions:

FULL SCALE 0dBm
ENTRY 100
FREQ 1MHz
LO DIST mode
0 dBm from tracking output or source

The signals given at test points on the System Functional Block Diagram found in the appendix were measured using the above test setup and a high impedance 10:1 probe. The setup conditions are also noted on the block diagram. Normal troubleshooting techniques used in this manner will allow isolation to a service group without having to put any of the modules on an extender board. Once the service group is discovered which is causing the problem, the appropriate functional block diagram for the service group may be used to isolate the problem to the board level.

NOTE

As the technician gains experience in the repair of the 3586, the functional block diagrams contained throughout the manual become the most often used pages. All troubleshooting to the board level should be done using the functional block diagrams at the end of each service group. Note that the functional block diagrams have parts locators with the test points used clearly identified by a star and arrow. If a star on a functional block diagram has two arrows originating at the same star it means that the test signal measured is the same at both points. Once down to a board in a service group the actual schematics may be used. Remember that the System Functional Block Diagram found in the appendix is a very useful aid in isolating down to the service group level.

8-11. SERVICE VOLUME ORGANIZATION

8-12. The service information in this volume is divided into four sections: 1) Turn-On Initialization and "Milking The Front Panel"; 2) Troubleshooting; 3) Detailed Functional Description; and 4) Service Groups. An appendix is included at the back of the manual and contains a Mnemonic Dictionary, plus duplicate copies of the 3586 Major Signal Chart and Turn-on Troubleshooting Flowchart. A copy of the System Functional Block Diagram is also included. Refer to paragraphs 8-13 through 8-19 for outlines describing the content of each section.

8-13. Turn-on Initialization and Milking the Front Panel (Section Outline)

8-14. The information contained under this heading is described briefly and organized as shown below:

1. Unique Terminology - covered here are terms used throughout the manual which describe unique modes and operating conditions of the 3586.

2. Turn-On and Calibration - explained here is how the instrument should respond at "turn-on" and the CALibration cycles available to the instrument. Also included under this heading are the instrument's Calibration Error Codes and Mode Error Codes.

3. Milking The Front Panel - Following a successful turn-on, (no failures), this subtopic explains ways of milking the front panel for additional information concerning an instrument malfunction. Included under this heading are the procedures for accessing the front panel Self Tests (Test/Functions).

8-15. Troubleshooting (Section Outline)

8-16. The information contained under this heading is described briefly and organized as shown below:
1. General Troubleshooting - troubleshooting alternatives based on the technician's familiarity with the instrument.

2. Troubleshooting Guidelines - generalized hints that the technician should keep in mind while troubleshooting the 3586A/B/C.

3. Primary Troubleshooting - provides information whereby a basic determination can be made as to whether the processor, the receiver, or the power supplies are causing improper instrument operation.

4. Troubleshooting Hints - hints that are intended to simulate what a technician experienced with the 3586A/B/C would give as advice for fixing a specific malfunction.

5. Major Signal Troubleshooting — procedural checks to establish a measure of confidence for the technician as to the status of key internal signals in the instrument.

8-17. Detailed Functional Description (Section Outline)

8-18. The information contained under this heading is described briefly and organized as shown below:
1. Block Diagram Description - brief description of the instrument's purpose plus a functional overview of the operation of the instrument using the system block diagram.

2. Detailed Functional Description - explanations of the individual circuits contained in 3586A/B/C instruments.

8-19. Service Groups (Section Outline)

8-20. The service groups consist of schematics, component locators, functional diagrams, and troubleshooting procedures for one or more related circuit boards. Included at the beginning of the service group section is an explanation of what service groups are and how to identify them. The service groups are arranged in the following order:

1. Signal flow
   a. Input (A)
   b. IF/Audio (B)
   c. Digital Process and Display (C)

2. Support and Optional Functions:
   a. Step/Sum Loops (D)
   b. Fractional-N Loop (E)
   c. Calibration (F)
   d. Impairment Measurement (G)
   e. Reference Oscillators (H)

3. HP-IB (I)
4. Power (J)

Table of Contents

8-21. TURN-ON INITIALIZATION and MILKING THE FRONT PANEL

8-22. The goal of this section is to provide servicing personnel with information on how a 3586A, B, or C should respond when power is applied, and how to "exercise" the front panel as a means towards identifying the cause of instrument malfunctions. Problems in the 3586 can often be isolated to a circuit board level by using internal self tests and interpreting front panel results.

8-23. For the technician who is unfamiliar with the instrument or if the instrument malfunction is not clearly defined, it is recommended that he/she review the topics contained in this section before proceeding to the Troubleshooting section.

8-24. A technician who is very familiar with the instrument may wish to use the Turn-On Troubleshooting Flowchart (Figure 8-3) at the end of this section or proceed to Troubleshooting Hints in the next section.

8-25. 3586 Unique Terminology.

8-26. Throughout Section VIII (Service), some terms describing unique modes or conditions of the 3586 are used frequently. These terms are defined as follows.

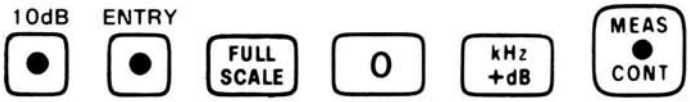
FULL SCALE — The Full Scale setting of the instrument is the number of dB referenced by Ø on the front panel meter. It also represents the upper limit of input signal level in dB that can be measured by the True RMS to DC Detector/Logger circuits without distortion beginning to occur. The Full Scale setting together with AUTO/ENTRY, 10/100dB RANGE selections determine how much gain or attenuation will be applied to the input signals to obtain the proper input level for linear operation of the Detector/Logger circuits. When AUTO 10 or AUTO 100 are selected, the instrument is allowed to AUTO-RANGE (i.e select its own Full Scale setting according to the largest signal present at the input to the instrument). When ENTRY 10 or ENTRY 100 are selected, the operator manually enters the desired Full Scale setting which then remains fixed.

RANGE — The operating range, 10dB or 100dB, of the IF Detector/Logger circuit on A21. When 10dB is selected, the entire linear input of the Detector is used to measure from the current Full Scale setting (upper limit) to 10dB below that setting (lower limit) providing amplitude measurement readings with 0.01dB resolution. When 100dB is selected, the same detector range must cover up to 100dB below the Full Scale setting and therefore only 0.1dB resolution is obtained.

AUTORANGE — A term used to describe the Controller's ability to choose its own Full Scale setting automatically. The processor receives an indication of broad-band power level from the A4 board and chooses the next 5dB increment higher than that value as the Full Scale setting. Depending on whether 10dB or 100dB Range is selected, different combinations of gain or attenuation are ordered from the RF and IF sections of the instrument by the processor to control the detector's operation over its most linear operating range.

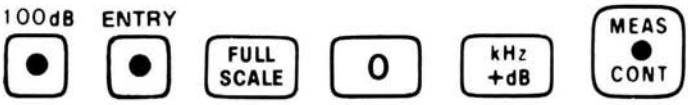
ENTRY 10

Use of this term is telling the operator to select the manual (ENTRY) method of entering a Full Scale setting and to select the 10dB Range for the Detector/Logger circuit on A21. Usually, the Full Scale setting entered by the operator is the next 5dB increment higher than the highest expected discrete frequency signal amplitude to be applied to the 3586 as an input. The key sequence for selecting ENTRY 10 is:



ENTRY 100

Same as ENTRY 10 except the 100dB Range of the A21 Detector/Logger is selected. The key sequence for selecting ENTRY 100 is:



AUTO 10

Use of this term is telling the operator to select the automatic (AUTO) method for determining Full Scale setting (processor-determined) and to select the 10dB Range for the Detector/Logger circuit on A21.

AUTO 100

Same as AUTO 10 except the 100dB Range of the A21 Detector/Logger is selected.

TURN ON CONDITIONS

When the 3586 is first turned on and after the automatic self-test and calibration cycle is completed, the instrument is in the "turn-on configuration". This configuration includes the following automatic selections and settings (no input signal applied):

AUTO CAL on, AUTO 10, AVE off, dBm, OFFSET off, CARRIER, USB, COUNTER off, LO DIST mode, 10k ohm, 1MHz, FREQ STEP = 1Hz, Full Scale = 120, Threshold = 0dBm, Time = 5 minutes, FREQ TUNE off, 3100Hz.

Whenever RECALL and then 0 are pressed, the 3586 will return to the preceding turn-on conditions without having to cycle the POWER switch.

MANUAL CAL

Manual (or Forced) Calibration is the procedure of causing the Calibration cycle to occur right away instead of waiting up to three minutes for Auto-Calibration to initiate it. If AUTO-CAL is off, just pressing AUTO CAL once will force an immediate CAL cycle to occur. If AUTO CAL is on and the three minute timing period is underway, pressing AUTO CAL twice will force an immediate CAL cycle to occur and then begin a new three minute timing period.

8-27. Turn-On and Calibration.

8-28. Pre Turn-On Verification. Before plugging the instrument into line voltage, verify that the power switch is in the STBY position and that the rear panel line switches are set for the proper line voltage. Next, apply the line power to the instrument and verify that the STBY lite on the front panel comes on. If the STBY lite is not on, check the line fuse for proper value and condition. If the line fuse is good, proceed to Service Group J and troubleshoot the +23V power supply.

8-29. Turn-On Initialization Sequence. What should the 3586 do at turn on? Well, if you are watching the front panel when the power switch is pushed to ON, you should see the following sequence of events. The total time to complete the sequence is normally about 9 seconds.

1. The instrument cooling fan should begin to run and the STBY lite should go out. All other front panel LED's should light including all segments of the seven-segment LED's, all annunciators (except STBY), and all key LED's.* (2.5 seconds.)

2. The condition of "all LED's lit" is replaced by the display sequence shown in Table 8-3. (6.5 seconds.)

Table 8-3. Numeric Display Sequence.

MEASUREMENT/ENTRY	FREQUENCY/ENTRY	Time Displayed***
blank	3586 X YY **	1.0 second
CAL	3586 X YY	2.2 seconds
CAL	1 000 000.0Hz	3.3 seconds
< -116dBm*	1 000 000.0Hz	(continuous)

Notes:
* Assumes no input signal.
** X = A,B, or C (Model number)
YY = OP if option 003 installed (A70 board -3586A/B only).
*** Time is approximate due to differing Controller clock frequencies.

NOTE

If the cooling fan does not run, check the line fuse for proper value and condition. If a good fuse (see Table 8-2) does not restore operation, set the power switch to STBY, proceed to Service Group J, and troubleshoot the input power. If the cooling fan runs but one of the following conditions exist, proceed to Primary Troubleshooting (paragraph 8-89):

a. The front panel indicators are all dark.
b. The CAL cycle did not complete successfully.
c. The front panel indicators are frozen in some condition.
d. The front panel indicators are continually cycling.

8-30. Instrument Calibration. During the turn-on sequence, a "turn on CAL" occurs in which the processor reads from ROM memory, writes into and reads out of RAM memory, and verifies correct operation of the display timing clock. It then calibrates the instrument in both WIDEBAND and LO DIST modes, at 1MHz, for all Full Scale settings from -35 to +25dBm. The processor stores away calibration constants for each setting, to be applied to all incoming signals.

8-31. A successful Turn-On and CALibration is indicated by the instrument noise floor (< -116dBm) displayed in the MEASUREMENT/ ENTRY area, and the initialization frequency of 1MHz displayed in the FREQUENCY/ENTRY area. Also, the following annunciators and key LED's are lit as the result of a successful initialization process:

Annunciators: dBm, CENTER, Hz
Keys: AUTO CAL, 10dB, AUTO, dBm, CARRIER, ⟋,
LO DIST, 75 (Rev. A) or 10k (Rev. B), 3100Hz

(See also paragraph 8-48.)

8-32. Additional Calibration Cycles. The Turn-On CALibration described above is one of four calibration cycles. The other three: AUTO-CAL, Manual (Forced) CAL, and Fast-CAL are explained below.

AUTO-CAL. AUTO-CAL is where the processor calibrates the instrument in the mode it's in, at the tuned frequency, for all Full Scale settings at timed three minute intervals.*

Manual (Forced) CAL. Manual (Forced CAL) is where the operator tells the processor through AUTO-CAL switch depression (or via HP-IB) than an AUTO-CAL cycle is desired now instead of at the next three minute interval.

Fast-CAL. Fast-CAL, which is commandable over HP-IB only, is where the processor calibrates the instrument at the tuned frequency for the presently selected Full Scale setting only. In addition, any time AUTO-CAL is ON and the operator changes the tuned frequency by 1MHz or more, or changes from any other mode to WIDEBAND mode, the AUTO-CAL cycle occurs at that time and a new three minute interval begins.

NOTE

Additional information on interpreting the various calibration modes and associated failures can be found in Service Note 3586A/B/C-3A. Refer to Section VII for instructions on obtaining this service note and for information on other available service notes.

8-33. Turn-On CAL Failures.

8-34. If both of the display areas immediately fill with the letter "r", the turn-on write/read test for RAM memory has failed. The problem is on the A60 board. The internal self-tests cannot be run under this condition. Proceed to Service Group C to troubleshoot the A60 board.

8-35. If the display area contains a single letter "d", the processor did not receive the interrupt clock signal from the display timing circuit. The problem is on the A60 board. Proceed to Service Group C.

8-36. LED Check.

8-37. After Completion of the RAM write/read test and the display timing circuit test which occur during turn-on Cal, the processor will momentarily light up all front panel LED's including all segments of the digital display areas. To locate and identify bad LED'S, perform

the Display Checks in Service Group C which allow a greater length of time to observe specific groups of annunciators and each digit individually.

8-38. Calibration Error Codes.

8-39. If the CAL cycle stops with a Calibration Error Code displayed in the MEASUREMENT display area, use Table 8-4 to determine the cause and the most likely area(s) where the problem could lie. Failure of any step in the CAL cycle is justification for running the two most significant internal self-tests (paragraph 8-48). A calibration error occurs when the number generated by the A/D converter, at the time the calibration signal was switched in, was not within permissable limits (± 3 dB of expected value). The CAL error format is CE-N where N is a number or letter as shown in Table 8-4. When all CAL errors occur sequentially, a break in the major analog signal path is suspect.

NOTE

Calibration errors are legitimate instrument failures and indicate a problem exists within the instrument.

Table 8-4. Calibration Error Codes.

Format is CE-N where N =	Item Under CAL	Suspect Cards
0 to 9,A,b	RF Gain, step N	A2*
C	400 Hz Filter	A10, A20
d	20 Hz Filter	A20
E	10/100 dB (or WIDEBAND)	A21, (A4) **
F	Weighted Filter	A21, A22, A70 ***

*If any RF Gain step fails, check the input attenuator on A2. Press MEAS CONT to exit the CAL cycle and run the internal analog self-test in paragraph 8-81 (TF13).

** If CAL is performed in WIDEBAND, the A4 BBP circuits are calibrated instead of the normal IF signal path through the A21 10/100 dB amplifier.

*** If A60S2(2) is OPEN and an A70 Impairments board (Option 003) is not installed, CE-F will *always* occur during the CAL cycle.

8-40. Mode Errors.

8-41. The 3586A/B/C continually monitors itself for correct operation and for proper selection and implementation of the many possible mode combinations. Detected malfunctions and operator errors are presented as error codes on the front panel in the MEASUREMENT/ENTRY display area. Refer to Table 8-5 to identify the cause of a displayed error code.

8-42. Operator Errors. An error code which was generated by an improper key depression by the operator may be cleared by depressing the MEASurement CONTinue key.

8-43. Instrument Failures. Some error codes indicate definite circuit malfunctions, while others indicate possible circuit malfunctions. Both cases provide direction in Table 8-5 to a specific service group for troubleshooting.

Table 8-5. Mode Error Codes.

Code	Definition
Err 1	Operator error. Attempt made to manually change the FULL SCALE while in AUTO range.
E 1.2	Operator error. Attempt made to select 10 dB range while in WIDEBAND or IMPULSE noise, or to choose ENTRY (Full Scale) while in Ø JITTER.
E 2.2	Ø JITTER selected and input signal level as measured at the output of the A21 "10/100 dB DC Amplifier" is 40 dB or more below Full Scale. Instrument failure is indicated if a valid signal is present at the input to A1. Perform Internal Self-Test TF13 (paragraph 8-81).
E 2.3	Ø JITTER selected and there is no 1 kHz (+ 60 - 40 Hz) tone present as determined by the A70 "Valid Frequency Detector" circuit. Instrument failure is indicated if a valid signal tone is present at the input to A1. Perform Internal Self-Test TF13 (paragraph 8-81). If TF13 passes, proceed to Service Group G and troubleshoot Ø jitter circuits.
E 2.9	Ø JITTER selected and the output of the A70 "Peak to Peak Detector" is not between −2 volts and Ø volts. Possible causes are: 1. Phase Jitter of test tone exceeds 40° p-p. 2. Failure of Phase Jitter circuits on A70. 3. Failure of A70 input to A22 board. Perform TF13 (paragraph 8-81) and, if it passes, proceed to Service Group G and troubleshoot Ø Jitter circuits (if phase jitter of signal tone is known to be less than 40° p-p).
E 3.N	One of the following loops is unlocked: N = 1 Second Local Oscillator (Service Group B) N = 2 Sum Loop (Service Group D) N = 4 Fractional N Loop (Service Group E) N = 8 Step Loop (Service Group D) A definite instrument failure is indicated. Proceed to the indicated service group for troubleshooting.
E 4.1	The Impulse counter did not start on command. Instrument failure. Proceed to Service Group G.
E 4.2	The Impulse counter did not stop after completing the selected time interval. Instrument failure. Proceed to Service Group G.
E 5	Operator error. Attempt made to manually change mode or frequency while in REMOTE, or; LOCAL key pressed while in LOCAL LOCKOUT.
E 6.1	Operator error. START pressed while Impulse Threshold is equal to or less than 60 dB below Full Scale.
E 6.2	Operator error. START pressed while Impulse Threshold is above the Full Scale.

Table 8-5. Mode Error Codes (Cont'd).

Code	Definition
Err 7	The Analog to Digital Converter was unable to make a conversion within two seconds. Instrument failure. If error code is constantly displayed, proceed to Service Group C and troubleshoot the A22 board. If it only flashes briefly, during a mode change, condition may be transient-related and acceptable as normal operation. (Note: A short on the −12V supply can also cause Err 7.)
Err 8	The Frequency Reference Loop is unlocked. Verify that problem is not caused by an invalid External Frequency Reference, then proceed to Service Group H and troubleshoot the A40 board. (See Note)
Note: "Err8" at turn on is normal if option 004 (internal oven) is installed. The Err 8 should go away after 15 seconds when the 3586 and the frequency reference obtain phase lock. Service Note 3586A/B/C-4 contains additional information on the "ERR 8" display. See Section VII for instructions on obtaining this service note and for information on other available service notes.	

8-44. Problems at Turn-On.

8-45. Power Circuits. Figure 8-3 is a flowchart designed to help the service technician handle the condition where the 3586 does not do what it is supposed to do when it is first turned on. The 3586 does not have a true "OFF" condition where input power is completely disconnected from all components in the instrument. It does have STANDBY (STBY) and ON as previously mentioned. In STANDBY, line power is applied to power transformer A99T1 and to the rectifier circuits. The +23VDC in the power supply (see Service Group J) is always available when the instrument is plugged in. This voltage is applied to the battery (A80BT1) charging circuit and also to the 10MHz Frequency Reference board (A16), if installed, to keep the reference oscillator oven warmed up and ready for immediate use. The other A99 rectified DC voltages (-23VDC, +-18VDC, and +8.5VDC) are applied to the voltage regulator circuits on A80 and only need a ground from the ON position of the POWER switch (A98S300) to supply regulated DC voltages of +-12VDC and +5VDC to the rest of the instrument. Failure of any of these circuits at turn-on will be immediately noticeable by failure of the 3586 to complete the turn-on initialization sequence. It is good, standard troubleshooting procedure to check power supply voltages as the first step in any troubleshooting sequence. See Service Group J for power supply checks.

8-46. Milking The Front Panel.

8-47. Before making a final decision as to what troubleshooting strategy will be used on a malfunctioning instrument, the service technician should determine if any additional information can be gained from "milking" the front panel operational controls. If the 3586 has undergone a successful turn-on sequence (paragraph 8-31), the technician can activate several instrument self tests via the front panel. These internal self tests (designated as Test/Functions, TF) are built into the instrument software and can verify functional operation of the instrument's circuits and assist in troubleshooting specific problems. Instructions for accessing, and detailed descriptions of the tests are given beginning at paragraph 8-49.

8-48. Operational Confidence Check. Following a successful turn-on sequence, a check of the overall operational status of the 3586 can be obtained by running internal self tests TF13 and TF14. The tests (one digital, one analog) take only two minutes to perform (with no

failures), yet they can tell the technician a great deal about instrument performance. If successful testing (all PASS) of these two functions is obtained, basic 3586 operation is probably normal (barring intermittant failures and/or temperature problems) and known problems may be pursued by proceeding to Troubleshooting Hints in the next section. Refer to paragraphs 8-81 and 8-82 for procedures on running these two tests.

8-49. Internal Self-Tests.

8-50. The 3586A/B/C has built-in self-test capability that can verify functional operation of a very large portion of the instrument circuits. In addition, there are several general purpose functions and capabilities that can be called upon to assist in troubleshooting specific problems.

8-51. The internal self-tests are accessed by a four-key sequence entry. These entries are either [RECALL] , [.] (decimal point), [CNTR→FREQ], N or else [RECALL] , [.] (decimal point), [RDNG→OFFSET] , N where "N" is a number key.

8-52. For ease of referral in later paragraphs, the individual tests/functions have been assigned a Test/Function (TF) numeric designator. Table 8-6 is a condensed listing of these tests/functions for quick reference by those familiar with their use. A more detailed description of each one is contained in the following paragraphs. Details for use of each test/function capability are contained in the specific service groups where they are most useful for troubleshooting.

8-53. Test/Function Capabilities.

8-54. The following set-up provides a good starting point for most of the test functions. Select ENTRY (FULL SCALE) and 100 dB (RANGE). Turn AUTO CAL OFF. Enter a Full Scale setting of −35 dBm.

8-55. TF1. Key sequence to activate is [RECALL] , [.] , [CNTR→FREQ] , [0]. This function may be used, after deactivating AUTO CAL, to clear out (set to zero) all of the calibration constants stored in memory after the last calibration cycle. The operator may then view the exact gain of the instrument (uncompensated) by activating either TF2 or TF12.

NOTE

Another way to zero the constants is to disconnect cable W1 between A4 and A2 and force a CAL. When unable to CAL (signal error >3 dB), the A60 processor sets the constants to zero.

8-56. The CALibration cycle can correct for amplitude errors in the analog signal path of the instrument for up to + −3dB. An instrument which is a borderline failure can be identified using TF1. As mentioned in the paragraph above, TF1 zeros out the current set of calibration constants so that the technician can view the actual gain of the instrument. In order to view the gain, first turn AUTO CAL off and then activate TF1. Next, either activate TF2 to use the precision CAL signal or use a calibrated external source to provide an accurate input signal (e.g., 1MHz at -40dBm). The level reading displayed, subtracted from the precision input, yields the gain or attenuation error of the analog signal path. For example, if a precise −40.00dBm signal is input to the instrument after the CAL constants

are zeroed out, and the measured amplitude reading is −42.87dBm in AUTO 10, the analog signal path is attenuating the input signal (a fixed loss) by 2.87dB. This is a large measurement error but it is still within the calibration compensation range (±3dB) of the 3586.

However, this hypothetical example would indicate significant signal degradation exists and suggests that one or more components may have changed value due to temperature, stress, shock, or some other reason. If the degradation continues until the error exceeds 3dB, the instrument will fail CAL and will need additional repair.

Table 8-6. Test/Function Capabilities.

Paragraph	T/F Desig	Key Seq*	Test/Function	Exit**
8-55	TF 1	CF, Ø	Clears CAL constants	---
8-58	TF 2	CF, 1	Tracking CAL signal ON Input signal OFF	TF 3
8-66	TF 3	RO, 1	Input signal ON Tracking CAL signal OFF	---
8-67	TF 4	CF, 2	Hundredths digit ON	TF 5
8-68	TF 5	RO, 2	Hundredths digit OFF	---
8-69	TF 6†	CF, 3	First L.O. 1000 point sweep	MC
8-70	TF 7	CF, 4	RF Gain, 12 step cycle	MC
8-73	TF 8	RO, 4	−12 volt supply and A/D check (−125.50 to −130.30)(X.0938) Range -120dB	PWR
8-74	TF 9	CF, 5	IF GAIN, 22 step cycle	MC
8-77	TF 10	RO, 5	Right # = A/D converter offset Left # = Offset/Input difference	MC
8-78	TF 11	RO, 6	Display Scan Rate (100 ± 10 Hz)	MC
8-79	TF 12	CF, 7	1 MHz CAL signal ON Input signal OFF	AC
8-81	TF 13	CF, 8	Receiver Test 1.0-1.11 RF Gain 2.0-2.13 IF Gain 3.1-3.2 Detector/Counter 4.1-4.32 Flatness 5.0 Audio	MC
8-82	TF 14	CF, 9	Digital Test 10 dB ROM A (U12) 100 dB ROM B (U11) AUTO ROM C (U10) ENTRY ROM D (U9) AVE ROM E (U8) dBm ROM F (U7) (other) RAM	MC

* All key sequences include RECALL, • (decimal point) first.

CF = CNTR→FREQ RO = RDNG→OFFSET

** MC = MEAS CONT PWR = Cycle POWER switch AC = AUTO CAL

† Available in Revision "A" ROM software only.

8-57. If AUTO CAL is now turned on, with the reading of -42.87 dBm present, the reading should correct to −40.00dBm. This would show how the instrument has stored a calibration constant of +2.87dB which it will add to all incoming signals as long as it stays on the selected Full Scale setting and at the selected frequency. Other constants are stored for different full scale settings, but if the frequency is changed by more than 1MHz from the frequency at which the last CAL cycle occurred, calibration will automatically occur again.

8-58. TF2. Key sequence is [RECALL] , [.] , [CNTR→ FREQ] , [1]. This function provides a precision signal generator source for testing the analog signal path in the receiver input section by switching out the input signal at the front of the Input Amplifier (A2) and switching in the calibration signal from A4. This signal has the same frequency as shown in the FREQUENCY/ENTRY display. The amplitude of this signal is −40dBm for FULL SCALE settings of 0dBm or lower and −20dBm for FULL SCALE settings of +5dBm or higher. In addition, anytime CAL is selected, the A22 board switches in a CAL oscillator frequency to beat with the second I.F. signal (15.625kHz) and to produce an audio signal of 800Hz (3586A) or 1000Hz (3586B) to test the IMPAIRMENTS options on the A70 board. To exit this function, use TF3. (See also paragraph 8-79).

8-59. Frequency Response, Gain, and Signal Path Checks. Assuming that the instrument has completed the turn-on cycle (paragraph 8-31) with no failures, the technician has two possible methods of making additional front panel functional checks. Activating TF2 can provide a tracking CAL signal for checking any desired frequency or, the technician may elect to input a signal from an external source.

8-60. Whatever the source of the signal, first set up the 3586 to measure that signal at full scale. For example, if TF2 is used, select ENTRY 100 and enter a Full Scale setting of −40dBm (the CAL signal is −40dBm with this full scale setting). If an external signal is used, match the full scale setting to the amplitude of the input signal. By now changing the tuned frequency of the 3586 (TF2 used), the frequency response of the instrument may be checked (except for A1 which is bypassed). By changing the external source frequency (if used) and holding the tuned frequency constant, the 3dB bandwidth of the selected bandwidth filter may be checked. Switching bandwidths will verify all possible IF signal paths.

8-61. Changing the full scale setting with a constant test signal amplitude allows the technician to check different RF and IF gain configurations for the instrument (refer to the gain/attenuation tables in Service Groups A and B).

8-62. Changing measurement modes allows a check of certain other circuits/boards. For example, selecting WIDEBAND allows a check of the BBP signal path (see Figure 8-F-1). For a clean, single frequency input signal (or TF2), WIDEBAND signal amplitude should be about the same as LO DIST signal amplitude.

8-63. Switching between AUTO 10 and AUTO 100 checks the capability of the instrument to autorange correctly which exercises the BBP Overload/Underload detection circuits on the A4 board. If the mode is switched from LO DIST to LO NOISE, the Trip Point Reference circuits are also checked on A4. The signal amplitude should be about the same between AUTO 10 and AUTO 100 which would prove that the A21 Detector/Logger circuit is working in both 10 and 100dB ranges. When using TF2 and changing tuned frequencies, if the measured test signal amplitude is always about the same, it shows that the First L.O. signal is tracking correctly and the A15/A4 CAL signal path is functioning correctly.

8-64. By inputting an external signal and using COUNTER, the input signal frequency measurement path bypasses the A21 logger circuits and the A22 A/D conversion circuits. If the frequency COUNTER works, there is a good chance that an amplitude problem may be due to one of the bypassed circuits.

8-65. For checking the A1 board, an external 50 ohm or 75 ohm source can be used to check all of the input termination impedances. See paragraph 8-A-70 in Service Group A for impedance mismatch correction information. A frequency response problem can also be checked using an external source through the A1 board to see if it is the problem. If there is a frequency response problem using an external source but not when using the TF2 tracking CAL signal (see paragraph 8-60), A1 is probably bad.

8-66. TF3. Key sequence is [RECALL] , [.] , [RDNG→ OFFSET] , [1] . This function switches out the Tracking CAL signal (see TF2) and switches in the input signal at the front of the Input Amplifier (A2).

8-67. TF4. Key sequence is [RECALL] , [.] , [CNTR→ FREQ] , [2] . This function turns the hundredths digit ON in the amplitude display for comparison measurements in modes which normally only display amplitude levels to the nearest tenth of a dB. This function may be used anytime the RANGE selection is 100dB or WTD filter is selected. To exit this function, use TF5.

8-68. TF5. Key sequence is [RECALL] , [.] , [RDNG→ OFFSET] , [2] . This function turns the hundredths digit OFF in the level display anytime the RANGE selection is 100 dB or WTD filter is selected.

8-69. TF6. Key sequence is [RECALL] , [.] , [CNTR→ FREQ] , [3] . This function provides a 1000 point, sweep frequency generator capability. It begins immediately, starting at the existing first local oscillator frequency and stepping the first L.O. frequency 1000 times in increments equal to the FREQ STEP setting. The sweep is continuous, taking approximately 20 seconds to complete one cycle. A synchronization pulse is generated at the beginning of each sweep for scope applications and this pulse may be accessed at the SYNC test point (TP1) on the A60 Controller board. To exit this function, press [MEAS ● CONT] .

This function when used in association with a spectrum analyzer is useful for examining and adjusting filter shapes.

NOTE

TF6 is only available when ROM's with Revision A software are installed. See Service Group C for method of identifying Revision A ROM's.

8-70. TF7. Key sequence is [RECALL] , [.] , [CNTR→ FREQ] , [4] . This function steps through all 12 combinations of RF GAIN/ATTENUATION possible on the Input Amplifier (A2) board. The input signal remains connected and the function is cyclic, beginning at −40dB and incrementing in +5 dB steps to +15 dB. To exit this function, press [MEAS ● CONT] .

8-71. A2/A21 RF checks can be made using TF7 and following the procedure outlined below.

1. Using a 75Ω external source, input a 1MHz signal at −45dBm into the 3586 (75Ω termination).

2. On the 3586 press RECALL and Ø. Select LO DIST, ENTRY 100, and a full scale setting of −45dBm. Reselect 75Ω instead of 10kΩ if the instrument has Revision B software (paragraph 8-C-27).

3. Activate TF7.

4. The front panel meter should step from −60dBm to ØdBm (Full Scale) in 11 steps (12 levels) of 5dB each (RF00 to RF11).

5. Press MEAS CONT to exit TF7 at the end of the next cycle.

6. Repeat steps 1-5 for an input signal of −40dBm (Full Scale also −40dBm) and then again for −35dBm.

7. The results using −40dBm and −35dBm should be the same as for −45dBm.

NOTE

This test will not work exactly the same way for any other input/full scale levels. Use only the values given.

8-72. If the twelve 5dB steps can be clearly seen on the meter in the test sequence of paragraph 8-71, the technician knows that all of the switchable gain/attenuation stages on the A2 board are switching correctly and that the A2 board is providing a full 5dB change to signal amplitude for each step. Also, the A21 board is providing additional 5dB step changes for at least 3 full scale settings correctly. By contrast, if twelve steps are visible but are not in 5dB increments or, if the twelve steps are not uniform, the problem is on A2. If the steps are 5dB but start higher than −60dBm and end higher than ØdBm (Full Scale), the problem is most likely in one of the IF stages rather than on A2 since that is the only way increased gain can occur. If the range of the steps is from below −60dBm to below full scale, the problem could be signal loss in A1 or in the output buffers of A2 as well as an IF problem. See paragraph 8-74 for a way to check the IF section (TF9). Use Service Group A to troubleshoot a problem with A1 or A2.

8-73. TF8. Key sequence is [RECALL] , [.] , [RDNG→ OFFSET] , [4] . This function provides a confidence check of the A/D converter on A22 by selecting a fixed negative D.C. voltage off a voltage divider and converting it to a digital readout. If the readout is between −125.50 and −130.30, the technician knows the whole path from the A/D input multiplexer to the A/D counter output is working. Also, by multiplying the readout by .0938, a close (+ −250mV) approximation of the −12VDC regulated supply voltage is obtained. If the −12V supply is good, then by inference so is the +12V supply good since it is used as a reference for the −12V supply.

NOTE

The instrument must not have any input signal applied for this test to work. It also must either be in AUTO 10 or in ENTRY 10 with a Full Scale setting of -120dBm.

8-74. TF9. Key sequence is [RECALL] , [.] , [CNTR→ FREQ] , [5] . This function steps through all of the possible IF GAIN configurations for the A20 and A21 boards. The input signal remains connected and the function is cyclic, beginning at Ø dB and incrementing in +5 dB steps to +95 dB. It then checks two special configurations of +35 dB and +25 dB gain and then repeats the cycle. To exit this function, press [MEAS ● CONT] .

8-75. A20/A21 IF checks can be made using TF9 and following the procedure outlined below.

1. Using a 75Ω external source, input a 1MHz signal at −55dBm into the 3586 (75Ω termination).

2. On the 3586, press RECALL and Ø. Select LO DIST, ENTRY 100, and a full scale setting of −20dBm. Reselect 75Ω instead of 10kΩ if the instrument has Revision B software (paragraph 8-C-27).

3. Activate TF9.

4. The front panel meter should step from −85dBm to +15dBm in 19 steps (20 levels) of 5dB each (IF 00 to IF 19). The meter should then briefly jump to about −45dBm for IF 20 and then to −55dBm for IF 21 and then the cycle should repeat.

NOTE

This test will not work exactly the same for other combinations of input signal level and full scale settings. Use only the values given.

8-76. If the nineteen 5dB steps and the two other steps can be clearly seen on the meter in the test sequence of paragraph 8-75, the technician knows that all of the switchable gain stages on the A20 and A21 boards are switching correctly. It is also known that a full 5dB of gain is being provided for each step. By contrast, if all the steps are visible but are not exactly 5dB, the problem is either on A21 or in the 10/35dB output amplifier stage on A20. If the steps are visible but start at less than −85dBm and end at less than +15dBm the problem could be signal loss anywhere in the receiver section of the instrument. If the steps are all exactly 5dB, the problem is most likely not in the 10/35dB amplifier on A20 nor on A21 (unless the IF logger circuit offset is misadjusted). See paragraph 8-71 for a way to check the RF section. Use Service Group B to troubleshoot a problem with A20 or A21.

8-77. TF10. Key sequence is [RECALL] , [.] , [RDNG→ OFFSET] , [5] . This function is used to adjust the amplitude display accuracy (see paragraph 5-8). The right hand number is the raw A/D Converter offset that exists with the A/D input grounded. The left-hand number is the signal from the IF logger minus the offset. To exit this function, press [MEAS ● CONT] .

8-78. TF11. Key sequence is [RECALL] , [.] , [RDNG→ OFFSET] , [6] . This function shows the display scan rate. It should normally be 90-110 (Hz) although the instrument may work satisfactorily if the number is slightly outside this range. Symptoms of a slow scan rate would include slow display updating, slow audio test (TF13, group 5.0), slow measurement data sampling over HP-IB, slow turn-on initialization sequence, slow CAL cycle, etc. Symptoms of a scan rate that is too fast could include inaccurate measurement data sampling over HP-IB (only) due to insufficient settling times after switching transients have occured. To exit this function, press [MEAS ● CONT] .

8-79. TF12. Key sequence is [RECALL] , [.] , [CNTR→FREQ] , [7] . This function provides a constant 1 MHz CAL signal into the CAL input of the A2 board. The 1 MHz is an output of the A40 Frequency Reference board, gated through the A15 board as a substitute for the Tracking CAL signal. Use of this signal allows the first L.O. to be tuned around the 1 MHz CAL signal using the front panel frequency keys. In this way detailed checks can be made of the filter shapes. This function will be automatically exited any time a manual or automatic CAL cycle occurs.

8-80. A70 Circuits Check. Circuits on the A70 board (option 003) can be checked using TF12 as follows.

1. *Weighted Filter* - Press RECALL and 0. Activate TF12. Turn AUTO CAL off. Switch between 3100Hz and WTD 3100Hz. In 3100Hz, the 1MHz test signal should be about −40dBm. In WTD 3100Hz, the signal amplitude should drop about 2.3dB (3586A) or about 1.4dB (3586B). If it does, the Weighted filter works as does the Audio logger circuit on A70.

2. *Notch Filter* - Press RECALL and Ø. Activate TF12. Turn AUTO CAL off. In 3100Hz, the 1MHz test signal should be about −40dBm. Select NOISE/TONE (blue function key must be lit). If the signal amplitude drops about 60-70dB, the notch filter is working.

3. *Phase Jitter* - Press RECALL and Ø. Activate TF12. Turn AUTO CAL off. Select TONE (ENTRY FREQUENCY - SSB CHANNEL). Select ϕ JITTER (blue function key must be lit). If a residual phase jitter of less than .5°p-p is displayed, the phase jitter circuitry is at least functional.

4. *Impulse* - Press RECALL and Ø. Set THRESHOLD to −116dBm. Select IMPULSE (blue function key must be lit) and press START. If the impulse counter begins counting, the IMPULSE circuits are probably working.

8-81. TF13. Key sequence is [RECALL] , [.] , [CNTR→FREQ] , [8] . This function provides a confidence test of the main signal path through the receiver sections of the instrument. The test is similiar to the CALibration cycle in that the processor causes a calibrated test signal to be injected into the Input Amplifier (A2). With this signal present, the processor then selectively changes the instrument's analog signal path configuration (gain/attenuation step, filter selection, ect.) in a controlled sequence. As it does this, it compares the resulting signal value (amplitude or frequency) that it receives from the analog-to-digital converter (A22) against known values, with appropriate tolerances, stored in ROM memory. The test will stop at any step that fails (identifying same), which allows the technician to determine the failing portion of the instrument. There are five groups in the test sequence, with a PASS or FAIL indication for each step in each group. If all steps in TF13 fail, it indicates that a break in the main signal path through the receiver exists. Refer to paragraph 8-98 in the troubleshooting section. To exit this function, press [MEAS ● CONT] during the Group 5.0 repeat cycle.

Descriptions of the individual TF13 tests are given below and their failure directions are summarized in Table 8-7.

NOTE

It is possible, in some cases, for the instrument to fail portions of TF13 and still pass AUTO-CAL and also still meet all its performance specifications. This is true because CAL can compensate for analog signal path errors totaling up to ±3dB, while TF13 might reject a signal slightly less than 3dB in error. Rather than being contradictory, this situation provides useful information. It indicates that the instrument is marginally within specification and that further degradation may produce an out-of-tolerance condition. The principal value of TF13 is to help the service technician isolate a solid failure to a particular section of the instrument.

Group 1.0 to 1.11: The 1 MHz calibration signal (see TF12) is switched into the measurement signal path. Each of the 12 RF GAIN/attenuation steps from −40 dB to +15 dB is programmed, with the signal being checked for correct level at the detector for each 5 dB step. The 100 dB Range is used. Refer to Service Group A if any step from 1.0 to 1.11 fails.

Group 2.0 to 2.13: The 1MHz calibration signal (see TF12) is switched into the measurement signal path. Some of the IF GAIN steps are programmed, with the signal being checked for correct level at the detector for each step. Each of the switchable IF GAIN stages is checked for switching but all combinations of all stages are not checked. Refer to Service Group B if any step from 2.0 to 2.13 fails.

Group 3.1 to 3.2: Test 3.2 checks the counter (A22U6) for the correct reading of the signal frequency. Test 3.1 checks the 10 dB Range for a correct level at the detector of the 1 MHz signal at −40 dBm. Refer to Service Group C for failure of step 3.2 and Service Group B for failure of step 3.1.

Group 4.1 to 4.32: The tracking CAL signal (see TF2) is switched into the measurement signal path. This signal is stepped at 1 MHz intervals from 1 MHz to 32 MHz at −40 dBm. Flatness is tested by checking the level at the detector for each step using the 10 dB Range. Refer to Table 8-9 under "Frequency Measurements Incorrect" if any step from 4.1 to 4.32 fails.

Table 8-7. TF13 Analog Test Steps.

Group	Step(s)	Test Description	Troubleshooting Data	Service Group
1	1.0-1.11	RF Gain Test	Paragraph 8-A-14	A
2	2.0-2.13	IF Gain Test	Paragraph 8-B-25	B
3	3.1	10dB Detector Range	Paragraph 8-B-61	B
	3.2	Frequency Counter	Paragraph 8-C-17	C
4	4.1-4.32	Flatness Test	See Note	
5	5.0	Audio Test	Paragraph 8-B-62	B
Note: 1. If all steps of TF13 fail, proceed to paragraph 8-98.				

NOTE

If the flatness test (Group 4) in TF13 fails, the problem cannot be on A1 because A1 is bypassed for this test. It also cannot be past the A5 Input Mixer since the A5 output frequency is

always 50MHz (First I.F.). The problem, therefore, must be on A2 or A5, or must be due to a non-linear input to A5 from the First L.O. source (A51). One additional possibility is that the A4-derived calibration signal amplitude is non-linear. If the flatness test in TF13 passes but external input signals have poor frequency response (e.g., low frequency inputs at 0dBm measure 0dBm but high frequency inputs at 0dBm measure <0dBm), the problem is probably on A1. For any flatness problem, set up the 3586 for a Full Scale reading at the failing frequency, and then measure signal amplitudes as shown in Figure 8-A-7 (Service Group A).

Group 5.0: The finale from Beethoven's Symphony Number 9 is synthesized from memory by selectively switching the First L.O. frequency around the 1 MHz CAL signal. The function (TF13) repeats Group 5.0 until manually exited. Refer to Service Group B if any discrepancy in the audio is noted.

NOTE

Service Note 3586A/B/C-3A contains additional information on interpreting TF13 failure codes. See Section VII for instructions on obtaining this service note and for information on other available service notes.

8-82. TF14. Key sequence is [RECALL] , [.] , [CNTR→FREQ] , [9] . This function provides a confidence test of the digital sections of the instrument. The test gives a PASS or FAIL indication together with a displayed date of the latest version of ROM software. The test includes some fundamental read operations from ROM and write/read operations from RAM memory modules on the A60 Controller board. If FAIL is displayed, a lit key LED indicates the failed ROM (see Table 8-8). Refer to Service Group C for procedures to follow if a FAIL condition exists. Successful completion (PASS) of TF14 is required in order to run TF13 (paragraph 8-81). This is true because the analog self-test relies on a correctly functioning digital Controller to provide valid analog test results. (See also Paragraph 8-C-42.)

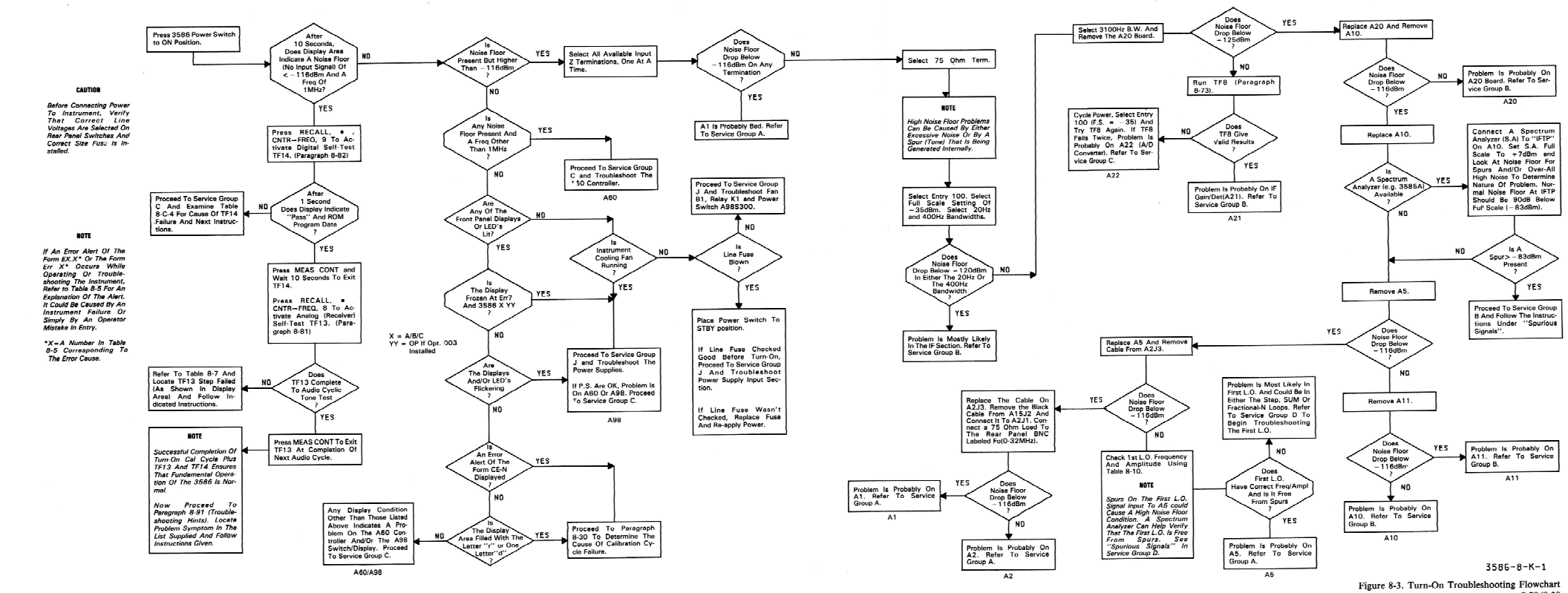
NOTE

The data displayed at the completion of this test identifies the ROM software revision where 7-23-79 is revision A and 6-30-80 is revision B.

Table 8-8. Digital Self-Test Failures.

Key*	Failed Module
10 dB	ROM A60U12
100 dB	ROM A60U11
AUTO	ROM A60U10
ENTRY	ROM A60U9
AVE	ROM A60U8
dBm	ROM A60U7

*Any lit key LED other than those listed indicates a possible faulty RAM.



3586-8-K-1

Figure 8-3. Turn-On Troubleshooting Flowchart

Table of Contents

8-83. GENERAL TROUBLESHOOTING.

8-84. The goal of this section is to define the problem and determine the assembly or assemblies that are the most likely cause of that problem. There will be occasional cases when a specific component is isolated as the probable cause (possibly by the self-tests). Most circumstances will point to several possible assemblies. The point is that different malfunctions will dictate different troubleshooting strategies and we highly recommend following the procedures of this section.

8-85. Unless the technician is very familiar with the instrument and has clearly defined the problem, it is desirable to review the contents under the heading "Turn-On Initialization and Milking The Front Panel." One should then proceed to the Troubleshooting Hints (paragraph 8-91). These hints will discuss the possible causes of the problem and refer to the appropriate service group(s) for detailed troubleshooting information.

8-86. A technician who is very familiar with the instrument may wish to use the troubleshooting flowchart (Figure 8-3) as a rapid isolation method for getting to the correct service group.

8-87. Troubleshooting Guidelines.

8-88. These are generalized hints that the technician should keep in mind while troubleshooting the 3586A/B/C.

1. Use the built-in self-tests that are described in the previous section. In some cases, these tests can lead directly to the problem area and in any case they can be used to eliminate possible problem areas if the test for that function passes.

2. The internal CALibration cycle provides valuable information also. Refer to the paragraphs on calibration (paragraph 8-30) for tips on how to use the CAL cycle to determine the operating status of many internal circuits.

3. Refer to the Block Diagram description (paragraph 8-105) for more background on the malfunction after referring to the Troubleshooting hints in paragraph 8-91.

4. Use "cool spray" to help isolate problems. Circuit cooler sprays are widely available and can be very helpful in isolating problems. The most generally used method is to spray selected components to see if the malfunction can be temporarily "cured". If this can be accomplished, the bad component is then isolated. This method will not work all the time, but it can be a great timesaver. It is especially helpful on "intermittent" problems which get worse with a rise in temperature.

5. Use signature analysis. The -hp- 5004A signature analyzer is an extremely powerful troubleshooting tool that allows a "window" on a digital node to give a go/no-go test. Without the analyzer, troubleshooting the digital sections of the instrument is difficult and requires much trial and error. If a 5004A is not available, keep in mind that most digital failures involve a line that is stuck high or low. Thus, a little guided probing using an oscilloscope in the suspected areas may find the problem.

6. Many problems on instruments that have been in service for awhile are directly traceable to corrosion. Often, simply removing and re-seating the affected printed circuit assemblies will "cure" a problem. Cleaning connector pins and/or switch contacts with an approved cleaning fluid is a permanent solution to many types of digital and analog circuit problems.

8-89. Primary Troubleshooting.

8-90. Primary Troubleshooting provides information whereby a basic determination can be made as to whether the processor, the receiver or the power supplies are causing improper instrument operation. Where necessary, branching to a service group will be indicated.

1. If the cooling fan runs when the power switch is ON but the front panel is dark, the +5 or +12 vdc regulated supply voltages may be shorted or out of tolerance. Proceed to Service Group J and troubleshoot the power supplies. If the supplies are working, check for a loose or open cable from the A60 board to the A98 front panel.

2. If at turn-on, the front panel indicators freeze at MEASUREMENT display = Err 7 and FREQUENCY display = 3586 x (where x = Model Letter A, B, or C), then the −12 vdc regulated supply voltage may be shorted. Proceed to Service Group J and troubleshoot the power supplies.

3. If at turn-on, the front panel indicators are flickering rapidly, there may be either a processor failure, excessive ripple on the +5 vdc regulated supply voltage, or supply voltage out of tolerance. Proceed to Service Group J and verify that the +5 vdc supply is free of any AC ripple and the supply voltages are correct before attempting to troubleshoot the Controller (processor) assembly in Service Group C.

4. If the instrument does not complete the automatic CALibration cycle at turn-on, it will present a failure indication in the MEASUREMENT display area. Proceed to Calibration Error Codes (paragraph 8-38) for definitions of failure codes.

5. If the instrument completes the CAL cycle successfully, but the noise floor appears excessive (> −116dBm at 1MHz), proceed to Service Group J and examine the +5 vdc regulated supply voltage for excessive ripple. If the +5 vdc is ripple-free, proceed to Troubleshooting Hints.

8-91. Troubleshooting Hints.

8-92. Introduction.

8-93. These hints are intended to simulate what a technician experienced with the 3586A/B/C, would give as advice for fixing a specific malfunction. To save time, they are referenced by malfunction. Find the malfunction description in the Troubleshooting Table of Contents that most closely fits the problem(s) experienced, then go to Table 8-9.

NOTE

Unless otherwise specified, the front panel instrument set-up for all procedures in Table 8-9 are those obtained at instrument turn-on. Pressing [RECALL] *and* [0] *will restore turn-on conditions when in doubt.*

Table 8-9. Troubleshooting Hints.

Problem	Procedure
AMPLITUDE MEASUREMENTS INCORRECT	1. Quick Reference for Amplitude Error Problems. a. Force a CAL cycle using the AUTO CAL key. If any CAL error codes are displayed (e.g., CE-A), proceed to the heading "CALIBRATION PROBLEMS" elsewhere in this table. If no CAL error codes are displayed, continue with b. b. If the exact symptoms of the amplitude error problem are **not** known, go to step 2. c. If the problem is known to be frequency-related, go to step 5 and check the first L.O. frequency at one of the tuned frequencies where the error exists. d. If the error exists at all frequencies and all Full Scale settings, go to step 9. e. If the problem exists only at certain Full Scale settings, go to step 8. f. If you suspect your source may be incorrect, go to step 13. 2. To troubleshoot an amplitude error problem, first determine the magnitude of the error and whether or not the error is related to frequency. Select ENTRY 100 and Full Scale setting of Ø dBm. Feed a Ø dBm signal into the 3586 at several frequencies, always making sure the output impedance of the source is correctly matched to the input termination impedance of the 3586. Try 20 kHz, 1 MHz, 10.333333 MHz, and 32.5 MHz. You can also try TF13 (paragraph 8-81) paying close attention to the amplitude readings during steps 4.1 to 4.32 of the test. If the amplitude reading is within ±3 dB of the input source at all frequencies (or ±3 dB of −40 dBm for TF13 group 4.1-4.32), then the instrument should be capable of compensating for this error by storing calibration constants for the frequency being measured during the CAL cycle. Force a CAL to occur at the frequency where the error occurs using the AUTO CAL key and repeat the amplitude measurement at that frequency. If the amplitude error disappears after CAL, the instrument is operating normally. If CAL errors occur (e.g., CE-A), refer to the heading "CALIBRATION PROBLEMS" elsewhere in this table. 3. If the CAL cycle is completed with no CAL errors, but an amplitude measurement error still exists afterward, check the first L.O. frequency using the procedure in step 5. If it is good, return here. If it is bad, proceed to Service Group D and troubleshoot the first L.O. If the first L.O. is good, a problem exists in the A2 switching relay, the Calibrator circuits (A4/A15) or in the Input Multiplexer (A1). To isolate the problem to A1 or A4/A15, try the following. Input a signal through different input terminations. If

Table 8-9. Troubleshooting Hints (Cont'd).

Problem	Procedure
AMPLITUDE MEASUREMENTS INCORRECT (Cont'd)	another impedance works, the problem may be in the A1 termination components, in the switching circuits on A1 or in the control of these circuits by the A60 processor (unlikely but possible). Remember to allow for impedance mismatch errors if your source does not have an equivalent output impedance. See Table 8-A-3 in Service Group A. 4. To check A1, bypass it by disconnecting the heavy black cable that normally goes from the rear panel Fo (0-32 MHz) BNC to A15J2 and connecting it to A2J1 (remove the gray/white/red cable on A2J1 temporarily). Now input a Ø dBm signal at 1 MHz from a 75 ohm source into the rear panel BNC (Fo). The 3586 should read +6.0±0.5 dBm at 1 MHz. If it does, the problem is on A1 (or in the gray/white/red cable). If it does not read +6 dBm, assuming a successful CAL was done first, then the A4 calibration signal is suspect. If incorrect, it would cause erroneous calibration constants to be stored during the CAL cycle and then to be applied to incoming signals. Refer to Service Group A for A1 problems and Service Group F for A4 problems. 5. If the amplitude error is greater than ±3 dBm at any frequency, CAL errors (e.g., CE-A) should be displayed during the CAL cycle. If CAL doesn't fail, the first L.O. may be at the wrong frequency. This would always keep the CALibration logic satisfied, since the first L.O. is used both to generate the CAL signal frequency and to tune the instrument. However, the instrument will not be tuned to the frequency that is displayed on the front panel if an error exists in the first L.O. frequency. Check the frequency of the Tracking Output at the rear panel BNC labeled Fo (0-32 MHz). If the Tracking Output signal (from A15) agrees in frequency with the frequency displayed on the front panel, then the first L.O. frequency is correct. If the amplitude of the Tracking Output is Ø±1.0 dBm regardless of frequency, then A15 is working correctly. If the problem is frequency-related and the first L.O. is good, go to step 9. If the Tracking Output frequency disagrees with the front panel tuned frequency, the problem is in the first L.O. and its digital inputs, or on A15. Verify the first L.O. frequency (Service Group D). If it is good, the problem is on A15 (Service Group F). If the Tracking Output frequency is good but the signal is low in amplitude, troubleshoot A15 (Service Group F). 6. If all measurements attempted on all frequencies are greater than ±3 dBm away from the input signal, the problem could be anywhere in the receiver section of the instrument, up to and including the A/D Converter (A22). 7. To help isolate the problem to a smaller area, try the following. Select different bandwidths to see if the problem is bandwidth-related. Also try WIDEBAND to bypass the entire IF section of the instrument. If WIDEBAND

Table 8-9. Troubleshooting Hints (Cont'd).

Problem	Procedure
AMPLITUDE MEASUREMENTS INCORRECT (Cont'd)	gives correct measurements, then A1, A2, A4 (Broadband power detection circuits only) and A22 are probably good. If not, then the problem should be in one of those circuits. To eliminate the A/D Converter (A22), run TF8 (paragraph 8-73) with no signals applied to the instrument. To eliminate the Input Multiplexer (A1) try bypassing it using the procedure outlined in step 4 above. 8. Feed a 1 MHz signal into the 3586 in AUTO 10 beginning at −60 dBm and increasing in 5 dB steps to +20 dBm. If the error occurs only on certain steps, then the problem is in one of the RF gain/attenuation stages on A2, or it is in one of the IF Gain stages on A20 or A21. On one of the failing steps, select WIDEBAND. If the measurement is now correct, the problem is in the IF gain stages on A20 or A21 (Service Group B). If the measurement is still bad, the problem is on A2 (Service Group A). 9. When the error is constant and it exists on all frequencies and all Full Scale settings or, when the error is frequency-related and the first L.O. is correct, then it is necessary to set up a given set of conditions and trace the signal level from board to board until it is lost or the amplitude error is found. 10. Select ENTRY 100 and a Full Scale setting of Ø dBm. Feed in a Ø dBm signal at 20 kHz. Remove the cable from A2J3. Disconnect the purple cable from A40J3 and connect it to A2J3. Connect a 50 ohm load to the 10 MHz BNC on the rear panel. Using a DVM on the load, you should read about 29 millivolts AC (−18 dBm on a Spectrum Analyzer such as the 3585A). If the output of A2 is correct, reconnect A2J3, remove the 50 ohm load and connect the purple cable to the IF TP jack on A10. Measure the signal at the 10 MHz BNC on the rear panel. It should read about 500 millivolts AC (with no load) on the DVM whenever a full scale signal is applied to the 3586 input (properly terminated). With a 3585 Spectrum Analyzer it should read +7 dBm at 15.625 kHz. If the A2J3 output is bad, the problem is in the input section (Service Group A). If the A10 test point output is bad but the A2 output is good, the problem is on A5 (Service Group A) or A10 (Service Group B) provided the first L.O. and second L.O. frequencies are good. (Refer to Table 8-8 to verify these frequencies.) If both outputs at A2J3 and A10 IF TP are good, the problem is probably on A20, A21 or A22. To check A22, perform TF8 (paragraph 8-73). If A22 is good, refer to Service Group B to check A20 and A21. 11. Another quick amplitude check is to connect a 75 ohm coax cable from the tracking output on the rear panel, labeled Fo (0-32 MHz), to the 75 ohm termination on the front panel. Tune the 3586 in 1 MHz steps from 1-32 MHz. The amplitude reading should be Ø ± 1.0 dBm for all frequencies. Select 10kΩ||50PF termination and repeat the steps from 1-32 MHz. At 1 MHz the amplitude should

Problem	Procedure
AMPLITUDE MEASUREMENTS INCORRECT (Cont'd)	be +6.0 ±0.5 dBm after CAL. As the frequency increases, the amplitude should gradually decrease until, at 30 MHz, it may be below +3 dBm. (It may be necessary to CAL at each 1 MHz step to see the decreasing amplitude levels.)
	12. If the 3586 and the source are not phase-locked together and amplitude errors only occur in the 20 Hz bandwidth, their respective tuned frequencies may be more than 10 Hz apart. Under this condition, CAL might complete its full cycle correctly. If this condition is suspected, use the 3586 counter in a wider bandwidth to determine the exact source frequency and tune the 3586 to that frequency for measurements.
	13. Verify your input source is correct by feeding the 75 ohm output into a 75 ohm load at 20 kHz and measuring the amplitude with a DVM. At Ø dBm it should read about 274 millivolts. A 50 ohm source into a 50 ohm load at 20 kHz/Ø dBm should read about 224 millivolts. Into a high impedance DVM with no load, it should read twice that or +6 dBm. If a spectrum analyzer is available, verify the source at higher frequencies, also.
AUDIO PROBLEMS	1. Verify that the audio is not bad because of signal processing problems somewhere else in the instrument (e.g., input section, IF section or local oscillators). One way is to measure a known signal (e.g., 1 MHz at Ø dBm) and see that the 3586 measures and displays its amplitude correctly.
	2. Turn up the volume control and see what the signal sounds like on the speaker. If a signal source is not readily available, run TF13 (paragraph 8-81) and listen to the Group 5.0 Audio test.
	3. If an audio problem does exist, it will usually be manifested as either weak, distorted or missing.
	4. Select the opposite sideband (erect or inverted) from that presently selected. If the audio is now good, the oscillator on A22 for the previously selected sideband (USB or LSB) is probably inoperative (Service Group C). If the audio is still bad, proceed to step 5 for a 3586A/B or step 6 for a 3586C.
	5. If the instrument is a 3586A/B with Option 003 (A70 Impairments board installed), remove A21. Change the STD/OPT switch (A21S1) from OPT to STD, replace A21, remove A70 and try the audio test again. If the audio is now good, A70 is probably bad (Service Group G).
	6. If the audio is still bad with A21S1 in STD and A70 removed (or the instrument is a 3586C), A21 and A22 are suspect. Refer to the audio troubleshooting procedures in Service Group B.

Table 8-9. Troubleshooting Hints (Cont'd).

Problem	Procedure
AUTO-RANGE PROBLEMS	1. Force a CAL cycle to occur. If CAL error codes (e.g., CE-A, etc.) appear, refer to the heading "CALIBRATION PROBLEMS" elsewhere in this table. If the CAL cycle is completed with no error codes displayed, fundamental operation may be assumed. 2. Determine all conditions that exist for the problem. Try with and without an input signal applied. Try AUTO 10 and AUTO 100 modes. Try LO DIST, LO NOISE and WIDEBAND. Try 3100 Hz and 20 Hz bandwidths. Try averaging (AVE) in AUTO 10 and AUTO 100. 3. If the problem only exists in AUTO 10, A21 is suspect (Service Group B). If the problem only exists in AUTO 100 or in both AUTO 100 and AUTO 10, A4 is suspect (Service Group F). 4. If the problem is related to averaging in LO DIST, AUTO 10, the A21 is suspect (Service Group B). If problem is related to averaging in LO DIST, AUTO 100, or to averaging in WIDEBAND, A4 is suspect (Service Group F). 5. Verify that your source input signal is not causing an auto-ranging problem through AM modulation. One way is to try a second source. Another way is to select ENTRY 100, Full Scale of Ø dBm, and input a signal at Ø dBm. If there is no "racking" of the amplitude display, then the input signal is probably not causing a problem. However, if the input had another frequency under 40 MHz present (e.g., Second Harmonic, spur, etc.) and *it* was racking in amplitude, it would cause the A4 board to command continuous auto-ranging from the A60 processor. 6. If steps 1-5 do not isolate the problem, try the following procedure to verify the gain selection configurations of A2, A20 and A21. Select ENTRY 10, LO DIST and 3100 Hz bandwidth. Force a CAL cycle to occur. Starting with a Full Scale setting +20 dBm, input a known signal of +20 dBm and look for a full scale indication on the meter and +20 dBm in the MEASUREMENT/ENTRY display. Simultaneously step both the Full Scale setting and the input signal downward, in 5 dB steps, to −80 dBm (or as low as your source can go in amplitude). At each step, the 3586 should display a full scale indication on the meter and should read the correct level of the input signal (± 1.0 dB) on the display. If it does not reflect accurate measurement on all full scale settings, note those full scale settings where it failed and refer to the Full Scale tables in Service Group B to identify the problem area. 7. Another possible cause of auto-range problems is a display scan rate. This is true because the display timing circuit on A60 also is used to control software delay routines for circuit settling times. Run TF11 (paragraph 8-78) to see if the scan rate is within its normal limits. If not, refer to Service Group C for A60 troubleshooting information.

Table 8-9. Troubleshooting Hints (Cont'd).

Problem	Procedure
AUTO-RANGE PROBLEMS (Cont'd)	8. Additional procedures which may apply can be found under OVERLOAD INDICATIONS in this table.
CALIBRATION PROBLEMS	1. Refer to paragraph 8-38 to identify the probable cause of CAL error codes displayed in the MEASUREMENT/ENTRY area on the front panel.
	2. If CAL fails every step in the calibration cycle, it signifies that a total receiver section gain error of $> \pm 3$ dB exists when the calibration signal from A4 is injected into the Input Amplifier A2. This could also occur if there is a break in the major analog signal path (cable disconnected or intermittent, etc.). Pinched cables, floating hardware, etc., may also cause the problem by shorting out the signal path.
	3. If the error code is CE-N where N=Ø-9,A,B then the problem could be anywhere in the receiver section of the instrument. Try running TF13 (paragraph 8-81) to see if the problem can be isolated to a particular area.
	4. Another possible cause of all CAL steps failing is the Calibrator signal itself. If the 3586 appears to measure input signals correctly but fails CAL, disconnect the black cable from A15J2 and connect it to A2J2. Connect a 75 ohm feed-thru termination (-hp- Model 11094B) to the rear panel BNC labeled Fo (0-32 MHz) and then connect a 75 ohm source set for 1 MHz/ -40 dBm to the feed-thru. Press RECALL and Ø on the 3586 front panel to restore turn-on conditions. Activate TF2 (paragraph 8-45). If the front panel display now reads about -40 dBm, A4 or A15 are suspect (Service Group F). (If a 75 ohm feed-thru is not available, the same test should indicate about -34 dBm.)
	5. Error code CE-F will always occur anytime the A60S2 switches are selected for Option 003 and an A70 Impairments board is not installed or is not fully seated. Refer to Service Group C for A60S2 switch selections.
	6. To check A4 without removing the instrument cover, first establish turn-on conditions (RECALL/Ø). Select ENTRY 100, turn AUTO-CAL off, activate TF1 (paragraph 8-55) to zero the constants and then activate TF2 (paragraph 8-58). Change Full Scale settings in 5dB steps from -45 to $+25$ dBm. The display should read about -40 dBm with Full Scale settings from -45 to Ø dBm and it should read about -20 dBm with Full Scale settings from $+5$ to $+25$ dBm. If it does, A4 is working correctly and the analog signal from the Input Amplifier (A2) through the A/D Converter is also good. This check, however, does not verify frequency (see step 7).
	7. It is possible for the first L.O. (minus 50 MHz) to be running at a different frequency than the front panel displayed frequency. (They should be the same.) With this

Table 8-9. Troubleshooting Hints (Cont'd).

Problem	Procedure
CALIBRATION PROBLEMS (Cont'd)	condition, the instrument would appear to be calibrating correctly at all frequencies as long as the CAL signal amplitude was within ±3 dB of what the processor expected to see out of the A/D converter in CAL. When not in CAL, however, input signal measurements would be in error. If this condition is suspected, connect a counter to the rear panel BNC labeled Fo (0-32 MHz). The frequency at this point is the Tracking Output and it should agree with the front panel displayed frequency when the first L.O. frequency is correct. If they disagree, the problem is somewhere in the first L.O. (Service Group D) or in the Tracking Output (Service Group F).
	8. When TF2 is active and a CAL cycle is performed, the displayed amplitude should read exactly −40.00 dBm or −20.00 dBm (depending on Full Scale setting). If any Full Scale setting does not read exactly −40.00 dBm or −20.00 dBm, one gain/attenuation stage may be bad on A2, A20 or A21. See Service Group B for tables of Full Scale settings versus system configurations.
	9. Another possible cause of Calibration problems is a low display scan rate. Run TF11 (paragraph 8-78) to see if the scan rate is within its normal limits. If not, refer to the A60 troubleshooting procedures in Service Group C.
DISTORTION (HARMONIC)	1. In measuring distortion, it is extremely important that the service technician verify that he has a "clean" system. His distortion-measuring equipment, cables, set-up, etc. must not introduce distortion while he is trying to evaluate distortion in the 3586. A spectrum analyzer (S.A.) is excellent for measuring distortion in the 3586 provided the input range of the S.A. is always set 10 dB higher than the input signal. This keeps the S.A. internal distortion at Full Scale from introducing measurement errors. Also, use lowpass or bandpass filters to remove source harmonics from the input to the 3586.
	2. Harmonic distortion (HD) in the 3586 is both range and frequency dependent. 10.83 MHz is the maximum input frequency for which third-order HD (32.49 MHz) can be measured and 16.25 MHz is the maximum for second-order HD (32.5 MHz). This is due to the 32.5 MHz upper frequency limit of the 3586.
	3. Empirical data obtained during development showed worst case second-order HD is on the −10 dBm Full Scale setting at 16.25 MHz. No third-order HD was noted during 3586 development.
	4. If the HD is range-dependent (> 4dB between ranges) it is probably caused by the Input Amplifier A2. If not range-dependent, the Input Mixer A5 is suspect. Both A2 and A5 are covered in Service Group A.
	5. It is unlikely that HD can be caused by any circuit past the Input Mixer (A5) since the input signal has been converted to stable IF frequencies past that point.

Table 8-9. Troubleshooting Hints (Cont'd).

Problem	Procedure
DISTORTION (INTER-MODULATION)	1. Establish a "clean" measurement system as per step 1 under "DISTORTION (HARMONIC)" above. 2. Intermodulation distortion (IMD) usually occurs in one of two frequency bands based on separation of two input frequencies: 200 Hz - 3 kHz (low band) 20 kHz - 1 MHz (high band) 3. If the IMD occurs in the low band only, the problem is most likely on the A5 or A10 boards. If the IMD problems occurs at any frequency separation (high and low bands), try all of the possible Full Scale settings. If the problem is range dependent (i.e., only occurs on certain Full Scale settings) then A2 is probably bad with A5 as another possible suspect. If harmonic distortion is within specification, then A2 is most likely the problem area. 4. Refer to Service Group A for detailed troubleshooting of IMD problems.
FREQUENCY TUNING (RPG) INOPERATIVE	1. If the manual frequency tuning control (also called rotary pulse generator or RPG) is inoperative, the A98 Switch/Display RPG logic (and the RPG itself) are suspect (Service Group C). This assumes that keyboard frequency entries are accepted.
FREQUENCY MEASUREMENTS INCORRECT	1. Verify the frequency of your source using a counter or spectrum analyzer. Phase-lock your source to the 3586 for all frequency accuracy measurements. 2. Force the 3586 to CAL to be sure there are no other errors/problems. If CAL error codes are displayed (e.g., CE-A, etc.), refer to paragraph 8-38. If CAL is completed without any CAL error codes displayed, then measure several randomly selected input frequencies from your source to determine the nature of the problem. Use the counter on the 3586 to see what it thinks the input frequency is. 3. If CAL is successfully completed, it is still possible to have the 3586 tuned to a different frequency than is displayed on the front panel. This condition is possible because the first L.O. which determines the tuned frequency of the instrument, is also used on the Tracking Output board (A15) as the source of the calibrator signal frequency. 4. To verify the first L.O. frequency, connect a counter to the rear panel BNC labeled Fo (0-32 MHz) which is the tracking output (75 ohms) from A15. Phase-lock the counter to the 3586. Tune the 3586 to several frequencies that will exercise all of the loops (step, sum, fractional-N) in the first L.O. For example:

Table 8-9. Troubleshooting Hints (Cont'd).

Problem	Procedure
FREQUENCY MEASUREMENTS INCORRECT (Cont'd)	20 kHz 1 MHz 2.333 333 MHz 32.5 MHz At each frequency, the counter should read the same as the front panel display. If it does, the First L.O. is tracking and operating correctly. If a spectrum analyzer is used to look at this signal, its amplitude should be Ø ± 1.0 dBm for any frequency (50 Hz - 32.5 MHz). 5. If the first L.O. is incorrect (as determined in step 4 above) the problem could be that one of the three loops (step, sum, fraction-N) is locked to the wrong frequency. This could result from a failure of part of the circuitry for that loop or from an incorrect ÷ N code from the A60 processor due to an A60 failure. Service Group D has procedures for determining the cause of first L.O. failures. 6. If the problem is that the instrument has amplitude measurement errors at a specific frequency, see if it will CAL at those frequencies. Also, measure the tracking output at the rear panel BNC labeled Fo (0-32 MHz) to see if the L.O. is correct at that frequency. If not, see step 5 above. 7. If only the 3586 counter is incorrect, i.e., tuned frequency amplitude measurements are correct but the counter reads differently from the input signal, the A22 board is probably bad (Service Group C).
FRONT PANEL DARK	1. If the front panel is completely dark with AC power plugged in and STBY selected, check to see if the line fuse is the proper type and size and that it is not blown. Replace if necessary. If the new fuse blows also, proceed to Service Group J and troubleshoot the power supply. 2. If the fuse is good, press the power switch to ON. If the panel is still dark, see if the fan is running. If no, proceed to Service Group J and troubleshoot the power supply. 3. If the fan is now running and the front panel is still dark, the A60 board may not be fully seated or the cable between the A98 Switch/Display and the A60 Controller may be disconnected. Remove the top cover and check these items. 4. If all the boards are fully seated and the cables are connected, troubleshoot the power supply (Service Group J).
FRONT PANEL FLICKERING	1. If the front panel display has an unchanging presentation but is blinking or flickering, run TF11 (paragraph 8-78). If the display scan rate shown by TF11 is not within its normal limits (90-110 Hz), the problem is in the display timer circuit on A60 (Service Group C). If the display scan rate is normal, the A98 and A60 boards are suspect (Service Group C).

Table 8-9. Troubleshooting Hints (Cont'd).

Problem	Procedure
FRONT PANEL FLICKERING (Cont'd)	2. If the front panel display is changing randomly, the A60 processor may be receiving a constant reset command due to excessive ripple on the +5 vdc supply. Refer to Service Group J to check the +5 vdc supply. If the power supply is good, the A60 and A98 boards are suspect (Service Group C).
FRONT PANEL DISPLAY ERRORS	1. Errors in the information displayed on the front panel such as missing segments in digits, LED's not lit, incorrect LED's lit, etc., are most likely caused by A98 circuits. However, failure of some output circuits on the A60 Controller could also be a possible cause of this problem. Loss of some key codes may be caused by an open circuit on the A98 board. 2. Exercise as many modes, frequency combinations and key inputs as possible while noting all discrepancies observed. This will help to isolate the problem. Refer to Service Group C for troubleshooting the A98 and A60 boards.
HIGH NOISE FLOOR	1. If a high noise floor (> −116 dBm at 1 MHz) is present after the initial turn-on cycle is completed, the front panel can be "milked" to help identify the source and/or eliminate some circuits as possible contributors to the problem. 2. Select all available input impedance terminations, one at a time. If the noise floor drops below −116 dBm on one or more of the termination selections, the A1 board is probably bad (Service Group A). 3. Select the 20 Hz and 400 Hz bandwidths. If the noise floor drops below −120 dBm in either the 20 Hz or the 400 Hz bandwidths, one of two problems could exist. a. A spurious signal (SPUR), generated internally, might be present at a frequency 200 Hz - 1550 Hz away from the tuned frequency, or b. A20, where the bandwidth filters are switched in and out, could be bad. For both cases, Service Group B has additional troubleshooting information. 4. High noise floor problems can be caused by either excessive noise or by a spurious signal (SPUR) that is being generated internally. The best way of identifying which one is the problem is to connect a spectrum analyzer (e.g., 3585A) to the second IF (15.625 kHz) test point on the Second Mixer. You can do this by disconnecting the purple cable from A40J3 and connecting it to "IFTP" on A10. Then connect the 3585A to the "10 MHz" BNC on the rear panel. 3585A settings: Full Scale of +7 dBm, High Input Impedance, Bandwidth 3000 Hz. On the 3586, select ENTRY 100, 3100Hz bandwidth, and a Full

Table 8-9. Troubleshooting Hints (Cont'd).

Problem	Procedure
HIGH NOISE FLOOR (Cont'd)	Scale of −35 dBm. With no signal into the 3586, the noise floor should be greater than 80 dB below Full Scale on the 3585A or less than −73 dBm. If a signal is present it will be within 1550 Hz of 15.625 kHz. Refer to Service Group B and follow the instructions under "Spurious Signals" to isolate the source of the tone. 5. If the spectrum analyzer shows just a high over-all noise floor, the problem is most likely between the input connectors of the 3586 and the IF Filter Board (A20). To isolate further, proceed with step 9. If no problem is indicated by the spectrum analyzer, i.e., no spurs present and noise floor < −73 dBm, then the problem is most likely on the A20, A21, or A22 boards. To isolate further proceed with step 7. 6. If a spectrum analyzer is not available, first determine if the Detector and A/D Converter are capable of measuring a within-specification noise floor. (See step 7.) 7. Remove the IF Filter (A20). The 3586 should be in ENTRY 100, 3100 Hz B.W., with a Full Scale setting of −35 dBm. The 3586 front panel amplitude display should drop below −125dBm. If not, run TF8 (paragraph 8-73). If TF8 gives valid results, A21 is probably bad (Service Group B). If TF8 gives invalid results, try cycling the 3586 power switch and repeat TF8 (set-up front panel again in ENTRY 100 and Full Scale = −35 dBm). If TF8 still fails then A22 is probably bad (Service Group C). 8. If the noise floor is < −125 dBm on the 3586 front panel display with A20 removed, A21 and A22 are probably good. Replace A20 and remove A10. If the noise floor is > −116 dBm, A20 is probably bad (Service Group B). If the noise floor drops below −116 dBm with A10 removed, A20 is probably good. Replace A10. 9. Remove A5. If the noise floor is > −116 dBm, the A10 and A11 boards are suspect. Remove A11. If noise floor is still > −116 dBm, A10 is probably bad. If noise floor drops below −116 dBm with A11 removed, A11 is probably bad. Refer to Service Group B for both A10 and A11 troubleshooting. 10. If the noise floor is < −116 dBm with A5 removed, A10 and A11 are probably good. Replace A5. Remove the cable from A2J3. If the noise floor is > −116 dBm, A5 and the first L.O. are suspect. Check the first L.O. frequency and amplitude using Table 8-10. If a spectrum analyzer is available, check for spurs on the first L.O. by following the instructions under "Spurious Signals" in Service Group D. A5 is a more likely cause of the problem than the first L.O., therefore if a spectrum analyzer is not available, assume A5 is bad (Service Group A). 11. If the noise floor drops below −116 dBm with A2J3 disconnected, A5 and the first L.O. are probably good.

Table 8-9. Troubleshooting Hints (Cont'd).

Problem	Procedure
HIGH NOISE FLOOR (Cont'd)	Reconnect A2J3. Connect a 75 ohm load to the rear panel BNC labeled Fo (0-32 MHz). Disconnect the black cable from A15J2 and connect it to A2J1. If the noise floor is > −116 dBm, A2 is probably bad (Service Group A). If the noise floor drops below −116 dBm, A1 is probably bad (Service Group A). **NOTE** *In WIDEBAND, the normal noise floor is usually about −70 dBm or lower (no spec requirement). However, selecting WIDEBAND and seeing −70 dBm or lower does not guarantee that A1, A2, and A4 are automatically good when a high noise floor exists in LOw DISTortion. This is true because the lowest permissible full scale setting in WIDEBAND is −35 dBm and the 100 dB Range of the A4 logger circuit is automatically selected. Then, since broadband noise from Ø-32.5 MHz is normally so high (around −70 dBm), it would mask an out-of-spec noise floor (e.g., −90 dBm) in LOw DISTortion caused by A1, A2, or A4 and passed through a narrower bandwidth in the IF section.*
HP-IB PROBLEMS	1. Problems in communication over the HP-IB may often be attributed to improper set-up. Recheck your cabling, address switch positions, software addressing commands, etc. before assuming that a 3586 hardware malfunction has occurred. Also, if the mode switches on A62S1 are improperly selected, normal HP-IB operation is not possible. Refer to Service Group I for information on switch positions. 2. With the 3586 in LOCAL, disconnect the HP-IB interface cable and verify that the 3586 is completely functional from the front panel controls. 3. If the 3586 works correctly from the front panel and the system set-up for HP-IB operation is correct, but communication between an HP-IB "controller" and the 3586 cannot be established, refer to Service Group I for HP-IB troubleshooting information.
METER INOPERATIVE	1. If an input signal to the 3586 can be measured accurately on the front panel digital display, and/or the CAL cycle can be completed with no CAL error codes displayed, the signal which drives the meter is getting at least as far as the input multiplexer circuits on the A22 board. 2. Connect a digital voltmeter (DVM) to the rear panel BNC labeled METER. Select ENTRY 10 and a Full Scale setting of Ø dBm. Input a signal to the 3586 from a source at Ø dBm. The DVM should read Ø volts. Reduce the input to −10 dBm. The DVM should read −1 vdc.

Table 8-9. Troubleshooting Hints (Cont'd).

Problem	Procedure
METER INOPERATIVE (Cont'd)	3. If the DVM reads correctly for the test in step 2 above, the problem is either a bad meter or a failure in the Meter Amplifier circuits on A21 (Service Group B). 4. If the DVM reading is incorrect in the above test, the problem is probably on A21 or A22. Refer to Service Group B for additional information.
OVERLOAD/ UNDERLOAD INDICATIONS	1. When the 3586 is in AUTO 10 or AUTO 100, the operator normally will not have any visible indication of overload/underload conditions since the instrument will autorange to a new input configuration anytime an RF or IF overload/underload is sensed by the A60 processor. 2. If AUTO 10 or AUTO 100 are selected and the front panel OVLD annunciator is flashing, either the input signal is exceeding the maximum input level for proper operation of the instrument (+23 dBm) or the 3586 is not autoranging correctly. See AUTO-RANGE PROBLEMS in this table. 3. When ENTRY 10 or ENTRY 100 are selected, the operator must select the proper Full Scale setting to keep overload/underload conditions from occurring. Except for special operational circumstances (see paragraph 3-2-73), the normal Full Scale setting is chosen to be just above the input signal to be measured. If one of the three possible visible indications of an overload/underload condition exists under a normal Full Scale setting as described above, a problem is indicated. Visible indications include UL, OL or a flashing "OVLD" on the front panel. 4. If ENTRY 100 is selected and (for example) a Full Scale setting of Ø dBm is chosen for an input signal of Ø dBm, a flashing OVLD annunciator should not be displayed unless the input signal is increased to $> +1$ dBm. Be sure to select the correct Termination impedance. On the A4 board, the red LED should be lit anytime the OVLD annunciator is flashing. This signifies a front end (RF section) overload condition. It indicates to the operator that specification accuracy is not guaranteed under this condition since the A21 Detector/Logger circuit is not being operated in a linear portion of its operating range. An input signal $> +23$ dBm could also cause damage to the instrument if that is the reason the OVLD is flashing. 5. If the OVLD flashes anytime the input signal is less than .5 dB above the Full Scale setting, a problem is indicated. (This assumes there is only one signal being input to the 3586 and the 3586 is tuned to that frequency.) If the instrument CAL's correctly, proceed to Service Group F and troubleshoot the overload detection circuit on A4, followed by the A4 broadband power (BBP) detector. 6. There is no front panel display of a front end (RF section) underload condition in either ENTRY 100 or ENTRY 10.

Table 8-9. Troubleshooting Hints (Cont'd).

Problem	Procedure
OVERLOAD/ UNDERLOAD INDICATIONS (Cont'd)	However, by operating too far below full scale in ENTRY 100, the operator is deliberating accepting less accurate measurements (see Table 8-1 under "Level Accuracy" for the 100 dB Range). A front end underload condition exists anytime the input signal is less than −42 dBm and, in ENTRY 100, anytime the input signal is <7 dB below full scale. This condition can be verified by observing the yellow LED on A4. If it does not light when the input signal is < −42 dBm or when it is 8 dB or more below full scale in ENTRY 100 (and the instrument CAL's correctly), either the underload detection circuit or the BBP detector on A4 is probably bad (Service Group F). 7. In ENTRY 10, the A4 yellow LED (front end underload) should always be on if the source is <63 dB above full scale. This is because, in ENTRY 10, maximum attenuation (−40 dB) is applied to the input signal for all Full Scale settings from +20 dBm down to, but not including, a Full Scale setting of −55 dBm. This is in direct contrast to the three other selections (ENTRY 100, AUTO 100 and AUTO 10) where the RF gain/attenuation configuration is changed in 5 dB steps along with Full Scale setting changes. (See the tables in Service Group B that illustrate this relationship.) If the yellow LED on A4 is not lit when in ENTRY 10 and when the source is less than 63 dB above full scale, and the instrument CAL's correctly, proceed to Service Group F and troubleshoot the underload detection circuit and the BBP detector on A4. 8. In ENTRY 10, the red LED on A4 should light and OVLD should flash anytime the input signal is greater than 70 dB above full scale. If this does not occur, proceed to Service Group F and troubleshoot the overload detection circuit and the BBP detector. 9. Whenever the letters UL or OL appear in the MEASUREMENT/ENTRY display on the front panel, it indicates an IF underload or overload condition exists. UL or OL will normally occur in Entry 10 only. Although, during auto-ranging, UL or OL may be seen briefly in between changes in Full Scale settings, they should never be seen for more than an instant at a time. If either UL or OL is constantly displayed when AUTO 10 or AUTO 100 are selected, a problem is indicated in the level of the signal being applied to the True RMS Detector/Logger circuit on A21. That level is either too big (OL) or too small (UL) for the RF gain/attenuation and IF gain configuration being commanded by the A60 processor. It also means that the processor has already commanded the maximum gain possible in the IF section when UL is displayed (in AUTO) but the signal is still too small. If OL is displayed (in AUTO), it means that the least gain possible in the IF section has already been commanded by the A60 processor but the signal at the True RMS Detector/Logger on A21 is still too large. In either case, if an underload/overload condition of the front end (RF section) does not exist (both red and yellow LED's on A4 not lit), then one of the IF gain

Table 8-9. Troubleshooting Hints (Cont'd).

Problem		Procedure
OVERLOAD/ UNDERLOAD INDICATIONS (Cont'd)		stages on A20 or A21 may not be switching correctly (Service Group B). If an A4 LED is also lit (red or yellow), it may be an A2 gain/attenuation stage not switching correctly (Service Group A).
	10.	In ENTRY 10, it is normal operation to have UL displayed when the input signal is less than 17 dB below full scale. It is also normal, in ENTRY 10, to have OL displayed anytime the input signal is greater than 2 dB above full scale. If UL or OL are displayed when the input signal is >18 dB below full scale and <3 dB above full scale, a problem is indicated in either the IF gain circuits or the RF gain/attenuation circuits. Refer to step 9 above for troubleshooting information.
	11.	Since the A60 processor looks at the output of the A/D Converter on A22 to determine whether an IF overload/underload condition exists, there is a slight possibility that A22 could cause the display of OL or UL. Run TF8 (paragraph 8-73) to confirm A22 operation as normal or faulty.
	12.	When UL or OL are displayed under normal operating conditions, it means the input signal to the IF Detector/Logger on A21 is at a level that is outside the linear conversion range of the logger circuit. The operator should manually change the Full Scale setting to correct this condition.
RETURN LOSS PROBLEMS	1.	If the 3586 fails the performance test for Return Loss, the problem is most likely on the A1 board in the associated circuits for the particular input termination(s) that failed the test. If multiple terminations fail the test, there is a slight possibility that the input circuitry of A2 could be bad. Refer to Service Group A for troubleshooting information.

8-94. Major Signal Troubleshooting.

8-95. It is sometimes helpful to check some important instrument signals for level, frequency, and waveform when not enough information is available to adequately identify or categorize the problem. At such times, the technician would like to know just what is working in the instrument and what is not working. The major signal chart (Table 8-10) was constructed to provide some confidence in the over-all status of the instrument. The following procedural checks will give the technician an idea as to the status of key internal signals in the instrument. Also, if the major signal chart is used together with the 3586 System Functional Block Diagram (see appendix), problems not resolvable through standard troubleshooting techniques can often be quickly identified and isolated.

8-96. Before starting, remove the top cover and verify that the power supplies are operating at the correct voltages and are free from ripple. (Refer to Service Group J.)

8-97. Refer to Table 8-10. Using an oscilloscope, frequency counter or RF voltmeter (as appropriate), check each of the listed signals for correct level, frequency and waveform as indicated in the table. Disconnect all input signals before taking measurements. If any signal has an apparent discrepancy, or is not present at all, refer to the indicated service group for troubleshooting.

8-98. Total Analog Signal Path Failure.

8-99. Any break in the major analog signal path (i.e., from the front panel input connectors to the A/D Converter output) should be easily recognizeable. The instrument should fail all the CAL cycle steps and present all the CAL error codes (paragraph 8-38). If TF13 is also run, most or all of those tests (Groups 1-5) should fail also. Another possiblity for failure of all steps in TF13 occurs only with instruments having Revision B ROM software (see paragraph 8-C-27 for how to determine). If slow autoranging is selected by A60S2(7) being in the open (slow) position, *it is normal* for TF13 to fail all steps. Switch A60S2(7) must be temporarily set to the closed (fast) position to run TF13 for valid test results. See paragraph 8-C-32 for A60S2 switch selections.

Table 8-10. Major Signal Chart.

Signal	Location	Frequency*	Level*#	SG	Remarks
10 MHz OVEN (Option 004-A16)	Rear Panel	10 MHz (± 1 Hz)	3.5 volts	H	Sine wave (Jumper removed)
10 MHz (Reference)	Rear Panel	10 MHz (± 2 Hz)	2.5 volts	H	Sine wave
50 MHz (Reference)	Test Jack on A40 (J6)	50 MHz (± 10 Hz)	1.2 volts	H	Sine wave
2 MHz (Reference) NNI	Test Jack on A40 (J2)	2 MHz (± 1 Hz)	900 mV	H	Square wave-narrow width-positive pulses.
50-82.5 MHz (First L.O.)	Test Jack on A51 (J2)	A 51 MHz (± 10 Hz) B 82 MHz (± 10 Hz)	A 700 mV B 750 mV	D/E	Sine wave-Tracks front panel frequency (+ 50 MHz).
54-86 MHz (Step Loop)	Test Jack on A50 (J2)	A 54 MHz (± 10 Hz) B 86 MHz (± 10 Hz)	A 700 mV B 750 mV	D	Sine wave-2 MHz steps.
20-40 MHz (FRAC N)	Test Jack on A31 (TP1)	A 30 MHz (± 10 Hz) B 40 MHz (± 10 Hz)	A 2.0 volts B 2.4 volts	E	Sine wave
0-32.5 MHz (Tracking Output)	Rear Panel (Fo)	0-32.5 MHz (± 10 Hz)	1.4 volts	F	Sine wave-Tracks front panel frequency.
49.984375 MHz (Second L.O.)	TP1 on A11	49.984375 MHz (± 2 Hz)	1.3 volts	B	Sine wave-(use extender board to get at TP1).
15.625 kHz (Second I.F.)	IF TP on A10	15.625 kHz (± 2 Hz)	1.4 volts	B	Sine wave

* Frequencies and levels indicated A are with 1,000,000 Hz selected on front panel.

Frequencies and levels indicated B are with 32,000,000 Hz selected on front panel.

\# All measurements were taken with a full scale signal of 1MHz at ØdBm present at the 75Ω input. 3586 set to ENTRY 100, Full Scale = ØdBm, LO DIST mode. Input signal levels taken with 3586 tuned to 1MHz. All levels are in volts (peak-peak).

8-100. To troubleshoot a major analog signal failure, proceed as follows.

1. Remove the instrument top cover and verify all cables are properly connected.

2. Force a manual CAL cycle to occur, first in LO DIST mode and then in WIDEBAND.

3. If the CAL errors occur in *both* modes, the problem is probably on A2, on A22, or is due to a bad CAL signal from A4. These are the only items common to CAL in both modes. (See Figure 8-F-1 in Service Group F.)

4. Input a known signal (e.g. 1MHz at ØdBm) into the instrument (properly terminated) in the LO DIST mode.

5. If the signal is measured properly by the instrument, then the CAL signal is probably bad. If the input signal measures more than 3dB away from its actual input value, you can probably assume the CAL signal would work if it could get through the signal path. The problem now is most likely on A2 or A22.

6. Run TF8 (paragraph 8-73) to check A22. If bad, proceed to Service Group C and troubleshoot the A22 board. If TF8 is good, proceed to Service Group A and troubleshoot the A2 board.

7. If the CAL errors occur in WIDEBAND, but not in LO DIST, the problem is in the BBP signal path. (See Figure 8-F-1.)

8. If the CAL errors occur in LO DIST, but not in WIDEBAND, the problem is somewhere in the IF section. Activate TF2 (paragraph 8-58) or input a known signal from an external source. Then proceed to Service Group A to check the Input Mixer (A5) output signal. If it is good, proceed to Service Group B to trace the test signal the rest of the way through the IF section.

8-101. Frequency Problems.

8-102. For any 3586 that has been specifically identified as having a frequency measurement problem or even when the service technician would just like to verify frequency accuracy, the following procedure may be used to verify frequency measurements in the 3586.

1. Connect a frequency counter to the Fo (0-32MHz) tracking output BNC on the rear panel of the 3586.

2. Phase-lock the counter to the 3586 using either instrument as the reference.

3. Press RECALL and Ø to restore turn-on conditions.

4. The counter and the 3586 tuned frequency should both be 1,000,000.0Hz.

5. Step the 3586 tuned frequency in 1MHz steps from 1-32MHz. The counter should follow, ±.1Hz.

6. Tune the 3586 to the following frequencies, one-at-a-time, while verifying that the counter follows, ±.1Hz.

1,000,000.1Hz	1,555,555.6Hz
1,111,111.2Hz	1,666,666.7Hz
1,222,222.3Hz	1,777,777.8Hz
1,333,333.4Hz	1,888,888.9Hz
1,444,444.5Hz	2,000,000.0Hz

7. If any of the counter readings in steps 4, 5, and 6 are incorrect, the First L.O. signal has a problem. Proceed to service Group D to troubleshoot the First L.O. signal.

8. If the counter readings in steps 4, 5, and 6 are all correct, input a known frequency signal from an external source. (Verify the source frequency with the counter before insertion.) Phase-lock the source to the 3586.

9. Tune the 3586 to the same frequency as the source and turn on the 3586 COUNTER.

10. The 3586 COUNTER frequency should agree with the source frequency ±.1Hz. If it does not, proceed to Service Group C and troubleshoot the frequency counter circuits on the A22 board.

8-103. If the procedure in paragraph 8-102 is successful for all steps, the technician knows that the First L.O. frequency is completely functional for all frequency combinations from ØHz to 32,500,000.0Hz in 0.1Hz steps. This implies that the three loops (sum, step, and fractional −N) are also all working correctly as far as frequency tracking is concerned.

8-104. Other 3586 frequency problems could deal with USB/LSB oscillator frequencies (paragraph 8-C-18), CALibration frequencies (paragraph 8-F-22), or A70 CALibration Oscillator frequencies (paragraph 8-G-42). The reference paragraphs provide troubleshooting information in these areas.

Table of Contents

8-105. BLOCK DIAGRAM DESCRIPTION.

8-106. Understanding The Instrument.

8-107. The 3586A/B/C primarily measures telecommunications analog signals for correct frequency and signal level. Fold out the block diagram (Figure 8-8) at the end of this section located just in front of the Service Group Index TAB.

8-108. Major signal flow is from left to right and is indicated by the solid dark line at the top of the diagram. The 3586A/B/C is a dual-conversion, AM/heterodyne radio receiver with very accurate, digitally-controlled frequency selection between 50 Hz and 32.5 MHz. Specific signals selected for analysis are measured accurately with a true RMS detector/logger circuit. This level is then passed through an analog-to-digital converter to provide a digital display to the operator of the signal amplitude.

8-109. Functional Operation. One of the available balanced or unbalanced inputs in the 50 Hz to 32.5 MHz frequency range is selected via the Input Multiplexer (A1) and passed to the Input Amplifier (A2). A2 either amplifies or attenuates the input signal depending on its amplitude and passes it to the First Mixer (A5). A second input to A5, the first local oscillator (L.O.) signal of 50-82.5 MHz, comes from the Sum Loop VCO (A51). When the first L.O. frequency is mixed with the input signal, the first intermediate frequency (IF) of 50 MHz is obtained. The first IF signal is passed to the Second Mixer (A10) where it is mixed with the second L.O. frequency of 49.984375 MHz from A11 to obtain the second IF of 15.625 kHz. The IF Filter (A20) determines the final bandwidth of the second IF that is passed to the IF Gain/Detection board (A21). Additional amplification of the second IF is provided by A20 and A21 and the final signal level is then measured by a True RMS Detector/Logger stage on A21. The logarithmic DC voltage level from A21 is converted to a digital number by the Analog-to-Digital Converter (A22) and passed to the microprocessor on the A60 Controller board as the amplitude of the input signal. If the instrument COUNTER is on, the second IF signal also bypasses the detector circuits on A21 and the exact frequency is counted by the A22 board and passed to the processor. The processor then sends digital values for amplitude and frequency to the Switch/Display board (A98) for display to the operator.

8-110. Supporting circuits to the main signal flow include a stable frequency reference (A40), a very stable 10 MHz frequency reference (A16) which is Option 004, a tracking output generator (A15), a broad-band power (BBP) detector/overload detector/calibration signal generator (A4) and power supply (A80/A99). Also included are a sophisticated first local oscillator comprising seven printed circuit boards (A50,A51,A52,A53,A30,A31,A32) and a second local oscillator (A11). A telecommunications signal impairments board (A70) is available as Option 003 to provide additional audio measurement capabilities and A61 provides HP-IB interface as a standard feature of the instrument.

8-111. Grounding and Signal Isolation.

8-112. The 3586A/B/C has two levels of signal measurement grounds above chassis (mainframe) ground (see Figure 8-4). These are called "Isolated ground" (schematic symbol ▽ I) and "Signal ground" (schematic symbol ▽ s). Their purpose is to prevent "ground loops" present at low signal frequencies and to isolate the entire receiver input section from internally-generated spurs.

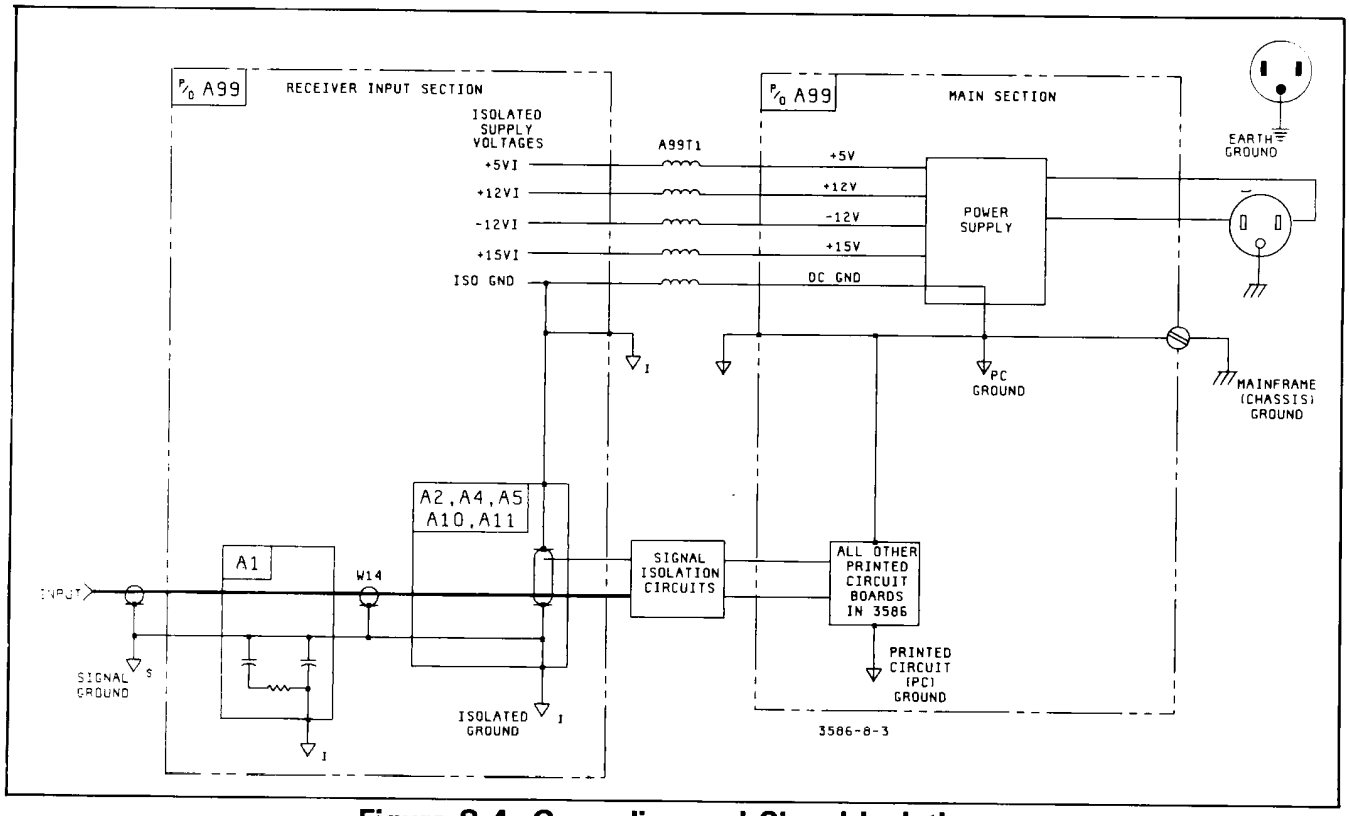


Figure 8-4. Grounding and Signal Isolation.

8-113. The receiver input section contains the A1, A2, A4, A5, A10, and A11 boards. The receiver input section common ground (Isolated ground) is separated from the remainder of the instrument circuit boards by isolation transformer A99T1 located on the motherboard (see Figure 8-4). On the A1 board, all grounds are Signal ground except power ground and relay logic ground which are Isolated ground. Signal ground is separated on A1 from Isolated ground by a resistor/capacitor network. Signal ground on A1 is tied directly to Isolated ground on A2 via the shield of connecting coaxial cable W14.

8-114. To preserve the ground isolation feature, all lines going between the isolated and non-isolated sections of the instrument must have isolated coupling. This isolation of signal, data and power supply lines is accomplished in various ways.

1. Isolation transformer A99T1 on the motherboard provides separation between "PC Ground" (schematic symbol ⏚) and "Isolated ground". It also isolates the power supply voltages used in the receiver input section (+15v, +12v, −12v and +5v). A99T1 acts as a saturable core reactor.

2. Photo isolator A99U1 separates the A60 Controller "DATA" line which provides relay logic for A1 and A2.

3. Pulse transformer A99T4 provides separation for the A60 Clock line (TCLK) which gates in the serial information on the DATA line to A1. Pulse transformer A99T5 does the same for the A60 Clock line (AMP CLK) to A2.

4. The first L.O. signal has a pi filter and transformer isolation on the first mixer board (A5).

5. Pulse transformer A99T3 separates the A60 "ISO LATCH" line from the A2 board.

6. Several DC Analog signal commons must cross the isolation barrier also and these all have resistive biasing for separation.

7. The dual Second I.F. signals obtain separation between the A10 and A20 boards by two Ground Isolation Amplifiers on the A20 board.

8-115. "PC Ground" (Printed Circuit ground) is the common signal and power ground for all circuits other than the receiver input section. It is connected to mainframe (chassis) ground by metal screws holding the motherboard to the mainframe.

8-116. Figure 8-4 functionally illustrates the grounding circuits present in the 3586A/B/C.

8-117. DETAILED FUNCTIONAL DESCRIPTION.

8-118. For the following detailed functional description of the individual circuits contained in the 3586A/B/C, refer to the schematic diagram of the specified PC board in the indicated Service Group.

8-119. Input Multiplexer - A1 (Service Group A).

8-120. The Input Multiplexer (A1) has three different circuit configurations depending on instrument model, 3586A,B, or C. For acceptable input level and frequency ranges for each balanced, unbalanced or bridged input, Refer to Table 8-1 Performance Specifications.

8-121. Telecommunication signals in the frequency range of 50Hz to 32.5MHz pass through the appropriate input jack and (if balanced) are converted to unbalanced signals. Frequency compensation is provided for balanced inputs and the correct termination impedance is supplied for all input selections by switching relays K1-K5.

8-122. Relay switching logic is supplied from the A60 Controller Board through photo-isolator A99U1 to the serial-to-parallel shift register U31. The data pulses are gated in to U31 by the termination clock signal (T CLK) from A60 through pulse transformer A99T4. Table 8-A-1 in Service Group A contains the A1 board relay configuration for each input termination selection.

8-123. Probe power comes from the −12VI bus and from a +15VI supply on the motherboard provided for probe power only (see Service Group J). "Isolated ground" is used as common.

8-124. Input Amplifier - A2 (Service Group A).

8-125. When the CAL cycle occurs, K1 is energized bringing the calibration signal from A4 into A2. This CAL signal is normally equal in frequency to the front panel frequency as seen in the FREQUENCY/ENTRY display. For frequencies below 20 kHz, CAL remains at 20kHz. However, if internal self-test function TF12 (see paragraph 8-79) is active, this calibration signal is a fixed 1 MHz.

8-126. When not in CAL, the input signal from A1 is passed through the de-energized contacts of K1 to the 0/20/40 dB Attenuator. K2 and K3 select the proper attenuation from this stage and pass the input signal to the amplifier. K4 controls the selection of a constant +5.25 dB or +15.25 dB voltage gain for the amplifier. FET Q1 provides high impedance buffering; U1a biases the FET and keeps the point between the emitters of Q3 and Q4 at virtual ground. Q2 ensures that Q1 inserts no additional losses by maintaining the Q1 source/drain loop at unity gain and also reduces distortion. Driving the same signal simultaneously, in-phase, through transistor pairs Q3/Q5 and Q4/Q6 has the effect of reducing distortion. The +5.25/+15.25 dB voltage gains are for a 3586A/B. The 3586C has gains of +0.25/+10.25 dB.

8-127. When U4(19) is HIGH, U1(7) turns on Q7 and 5dB attenuation is applied to the amplifier output. When Q7 is turned off, the signal is not attenuated and is passed directly to the Buffer amplifiers for output. The buffers provide a 50 ohm impedance output to the Input Mixer A5 and a 50 ohm output for broad band power measurements to the A4 board.

8-128. The ± 10.5 volt regulators add stability to the input amplifier. Current limiting protection is provided by R100,R110,CR5,CR6,CR8 and CR9.

8-129. Relay switching logic is supplied from the A60 Controller board through photo-isolator A99U1 to the serial-to-parallel shift register U5. The data pulses are gated in to U5 by the amplifier clock signal (AMP CLK) from A60 through pulse transformer A99T5. Table 8-A-2 in Service Group A contains the A2 board relay configuration for each gain/attenuation selection possible over the 55 dB gain selection range of the board.

8-130. The parallel eight bits from U5 are latched into U4 by the clock signal (ISO LATCH) from A60 through pulse transformer A99T3. Four of the outputs from U4 control relays K1-K4 through the open-collector drivers of U3. One of these U3(11) goes logic LOW when CAL is selected, energizing K1 to bring in the CAL signal from the A4 board and at the same time sending a (L) CAL signal to A4 to turn on CAL. Also, anytime a Full-Scale setting of +5 dBm or higher is selected, 40 dB of attenuation is required from the 0/20/40 dB circuits. Therefore, U3(13) goes logic LOW causing K3 to energize (K2 will de-energize) and 40dB is selected. This same LOW signal is applied to A4 to select the high level CAL signal of −20 dBm. (See Backdating section (Δ 2)).

8-131. As mentioned previously, U4(19) turns Q7 on or off to select 0 or 5dB attenuation to the input or CAL signal as required. The three remaining outputs of U4(2,5,6) select broad band averaging or set the proper threshold of the UL/OL trip points on the A4 board.

8-132. Input Mixer - A5 (Service Group A).

8-133. The first mixer A5 accepts 50Hz – 32.5MHz from A2 and mixes it with the first L.O. (local oscillator) frequency of 50 MHz – 82.5 MHz from the Sum Loop VCO (A51) to produce the first I.F. (intermediate frequency) of 50 MHz.

8-134. The 32.5MHz Low Pass Filter keeps frequencies greater than 32.5MHz from mixing with the first L.O. to produce a 50 MHz "image" I.F. For example, with 10 MHz selected the first L.O.would be 60 MHz and the difference frequency out of Balanced Mixer CR1 would be the desired 50 MHz. However, if a 110 MHz signal or spur were also present at the input, the difference frequency would also be 50 MHz (110-60) and an incorrect signal level would be present at the output of CR1 since the effect of the two signals (10 MHz and 110 MHz) would be additive.

8-135. Limiter U1 provides a strong drive signal for the first L.O. into Double Balanced Mixer CR1 to reduce both harmonic and intermodulation distortion.

8-136. The Balanced Mixer output signal is applied to a 50MHz crystal filter with a 10kHz bandpass. C23 is used to adjust a notch on the low side of the 50 MHz bandpass at 49.968750 MHz (50 MHz Minus (2 times the second IF of 15.625 kHz)). This notch provides image rejection for the second IF in the Second Mixer A10. A5Y1 and A5Y2 are a matched pair of crystals. A +14 dB amplifier compensates for signal loss in the mixer.

8-137. Second Mixer - A10 (Service Group B).

8-138. The second mixer A10 accepts the 50MHz first I.F. signal from A5 and mixes it with the 49.984375 MHz from the Second Local Oscillator (A11) to produce the second I.F. signal of 15.625 kHz.

8-139. The 50MHz crystal bandpass filter is used in conjunction with the same filter on the A5 board to produce a very steep-sided, 10 kHz wide bandpass signal into the second mixer. Crystals A10Y1 and A10Y2 are a matched pair. The notch adjust provides image rejection at two times the second I.F. signal.

8-140. Limiter U1 provides a strong drive signal for the second L.O. into Double Balanced Mixer CR1 to reduce intermodulation distortion and extraneous spurs.

8-141. U40 provides isolation and drive (+25dB) between the mixer and the two I.F. outputs. One output to the IF Filter A20 is 15.625 kHz with a 10 kHz wide bandpass, and the other output of 15.625 kHz has a 400 Hz wide bandpass obtained from the 400 Hz filter.

8-142. IF Filter - A20 (Service Group B).

8-143. The inputs to the IF Filter board A20 are two 15.625 kHz signals, one with a bandwidth of 10 kHz and the other with a bandwidth of 400 Hz. These two inputs pass through the "isolation barrier" separating the receiver input section from the remainder of the instrument. To keep unwanted spurious signals (spurs) from crossing this barrier also, each of the inputs is passed through a Ground Isolation Amplifier which has good common mode rejection characteristics.

8-144. The 3586A/B/C has three selectable bandwidths, 20 Hz, 400 Hz, or (depending on model and option) 1740/2000/3100 Hz. If the 20 Hz bandwidth is selected, the signal path

uses the 10 kHz wide signal input from A10, switches it through a 20 Hz Crystal Lattice Filter and passes it on to the A21 board through the wideband filter which has negligible effect on the signal.

8-145. If the 400 Hz bandwidth is selected, the signal path uses the 400 Hz wide signal input from A10 which bypasses the 20 Hz filter. This signal is also fed through the wideband filter which has negligible effect.

8-146. When the 1740/2000/3100 Hz bandwidth is selected, the 10 kHz wide signal input from A10 is used, by-passing the 20 Hz filter. When this signal is passed through the corresponding wideband filter, it receives the desired bandwidth (1740, 2000, or 3100 Hz). The output wideband filter stage provides an equalizing capability to square up the shoulders of the bandpass.

8-147. In order to achieve the steep sides desired (high Q) in the 20 Hz filter, two gyrator circuits are used to simulate the high inductance (2 Henries) required.

8-148. The two control lines, (H) 400 and (H) 1740/2000/3100, which select the second I.F. signal path, and a third line, (L) 35/(H) 10, which selects the gain of the 10/35 dB output amplifier are input under processor control from the A21 board.

8-149. IF Gain and Detection - A21 (Service Group B).

8-150. The second I.F. signal (15.625 kHz) is input to the A21 board from the IF Filter (A20) with a selected bandwidth of 20 Hz, 400 Hz, or 1740/2000/3100 Hz.

8-151. The 15.625 kHz signal is applied to a Ø dB or 35 dB (selectable) amplifier and then to a Ø dB-35 dB amplifier (selectable in 5 dB steps). The dynamic range possible therefore for IF gain is 70 dB on the A21 board, plus 25 dB through the output amplifier of the A20 board for a total of 95 dB.

8-152. In the Ø-35 dB amplifier (U8), a three digit code from the A60 Controller board is applied to the input lines of U4 (AØ, A1, A2) to select a pair of precision, thin-film resistors from U3. This selected resistor ratio establishes the gain for U8. R3 and R8 form a fixed −5 dB pad that always applies 5 dB attenuation to the signal.

8-153. The output of U8 (at TP1) is split three ways. One signal path goes through R32 directly to the A/D Converter (A22) where it is used to determine the exact frequency of the incoming signal to the instrument (Counter mode). Another signal path is through the logger stages to A22 for most amplitude measurements. The third signal path is to the Product Detector stage for demodulating the single sideband audio or (in CAL) for beating with the calibration oscillator signal from A70. The CAL output is used to check the Weighted filter in the A70 Impairments circuits (Option 003).

8-154. The Logger Range Expander and True RMS Detector/Logger circuits are mutually dependent for operation. The True RMS Detector/Logger can only accept a dynamic range on its input of approximately 50 dB. The expander circuit "expands" the logger range by compressing the 100 dB dynamic range output from U8 to a 50 dB range input for the Detector/Logger which, in turn, provides a constant current feedback path to help the expander circuit operate.

8-155. Whenever the 10 dB RANGE is selected on the front panel, the processor opens

switch U6d, turning on Q2 and switching in an additional 10 dB attenuator (R60, R61, and R62) at U9(2). The purpose of this additional attenuation is to cause the Detector/Logger to operate over the most linear portion of its characteristic curves for increased accuracy on the 10 dB RANGE.

8-156. The Detector Logger U5 takes the 15.625 kHz I.F. signal in at pin 1, computes the true RMS (root-mean-square) voltage level of the signal and provides a logarithmic DC output voltage at pin 6 that accurately represents the dBm level of the input signal to the instrument. In addition, when front panel averaging (AVE) is selected, the processor sets (H) SMOOTH high to turn on Q4. This shorts out filter capacitor C30 and allows greater signal averaging to take place using the larger capacitance of C29.

8-157. The 10/100 dB DC Amplifier amplifies the Logger DC output and provides proper output levels for the A/D Converter (A22). The output of U5 is temperature sensitive so compensation for temperature variations is provided by precision wire-wound resistor R20 and a network consisting of R9, R10, R11 and CR9. Also, the same processor signal that attenuates the Logger input by 10 dB in the 10 dB RANGE increases the gain of U10 to compensate for the attenuation by opening U6c. Because of the two different gain and offset configurations of U10, two sets of GAIN/OFFSET adjustments are provided; one set for the 10 dB Range and one set for the 100 dB Range.

8-158. The A/D Converter (A22) can only operate on negative input voltages. Therefore U20 clamps the output of U10 to a maximum positive voltage of 40 millivolts while allowing the negative voltage to swing as low as -5 volts.

8-159. Digital control of the IF circuits on the A20 and A21 boards is provided by the A60 Controller. A 16-bit serial data stream is clocked into serial-to-parallel shift register U1 and shifted into U21 until all 16 bits are in position (eight in U1 and eight in U21). The data is then latched into U2 and U22 and a new IF configuration is now selected.

8-160. The output data from U22 feeds a D/A Converter to provide the correct offset reference for the Meter Amplifier. This reference changes anytime a calibration cycle computes new error constants, thus making the front panel meter reading and the rear panel METER output more closely reflect the front panel MEASUREMENT/ENTRY readout.

8-161. In addition to the control signals already discussed, U2 outputs switch the gain of U7 between Ø dB and 35 dB, control the gain of amplifier A20U10 on IF Filter board A20, and control the selection of bandwidth (20 Hz, 400 Hz, or 3100/2000/1740 Hz) on the A20 board.

8-162. The Product Detector (U13) is a double-balanced mixer that accepts the 15.625 kHz bandwidth-limited IF signal from U8. This signal is mixed with the SSB LO signal from the A22 board to demodulate either the upper or the lower sideband audio. The SSB LO signal may also be from the A70 Impairments board if Option 003 is installed (3586A/B only) and CAL is active. This CAL signal would cause an 800 Hz (3586A) or 1000 Hz (3586B) audio tone to be output from U13 to specifically test and calibrate some A70 Impairments circuits during CAL. See Table 8-B-1 for the possible frequencies that can be input on the SSB LO signal line.

8-163. The output of U13 is fed through a Low-Pass Active Filter to filter out the carrier and the undersired sideband. The SSB Demodulated audio is then sent to the VOLUME control and the rear panel "AUDIO" jack if S1 is in the STD (standard) position. If Option

003 is installed, S1 should be in the OPT position and the audio is sent to the A70 Impairments circuits. Processed audio from A70 is then returned to A21 and now passes through the OPT contacts of S1 to the VOLUME control and AUDIO jack.

8-164. Analog switch U6a is normally closed except in CAL. When the CAL cycle is active, the (L) CAL line from A22 goes LOW, opening U6a and muting the speaker during CAL.

8-165. When CAL is not active, the SSB DEMOD audio is picked off the wiper of the VOLUME control and fed back to A21 where it passes through Audio Amplifier U16 to drive the speaker.

8-166. The Meter Amplifier is normally fed by the selected output of the Input Multiplexer circuit on the A22 A/D Converter board. The meter input signal passes through the closed contacts of A21U6b into the amplifier unless CAL is active. When the (L) CAL signal is LOW (CAL active), U6b opens, disconnecting the CAL cycle signal fluctuations from the meter. C49 acts as a "Hold" circuit, maintaining the last meter position that existed prior to CAL activation. S2 provides a special test capability (see Service Group B).

8-167. As mentioned above, the D/A Converter U23 sets the reference for the meter amplifier through U20b. This reference corrects the meter indication with the calibration constants obtained during the previous CAL cycle. U20a is a buffer amplifier for the rear panel "METER" jack with diodes CR6 and CR7 providing circuit protection. U20c keeps the meter from being over driven by limiting current flow through the meter.

8-168. Analog/Digital Converter - A22 (Service Group C).

8-169. The A22 board has three main functions: a Frequency Counter, a dual-slope A/D Converter, and sideband oscillators.

8-170. Frequency Counter. The IF INPUT from A21 is a signal that has been bandwidth-limited at 3100/2000/1740 Hz, 400 Hz, or 20 Hz around 15.625 kHz. This signal is limited by U4 to obtain a square wave input to the phase-lock loop (PLL) circuit. The purpose of the loop is to multiply the input signal frequencies by 20 to enable faster counting. If there are multiple signals in the channel, the loop locks on to the strongest one. U4d provides loop stability.

8-171. The output from the PLL is centered at 20 x 15,625 Hz or 312,500 Hz. By measuring the frequency of the second I.F. and by the A60 Controller knowing the frequency of the first L.O., the processor can calculate the frequency of the input signal and display it.

8-172. The A22 Logic State Machine (LSM) clears Counter U6 then gates the output of the PLL into the counter for one-half second. The processor then pulses (H) SCAN high and reads the value in the counter, one digit at a time, by reading output lines AD1, AD2, AD4, and AD8. The number in Counter U6 should be exactly one-half of the PLL output frequency or about 156,250 counts.

8-173. The ÷ 10 circuits (U14/U15/U16) accept 1 MHz from the A40 board and produce a 1 Hz reference signal and a 500 kHz counting signal (both square waves). The 1 Hz output establishes a one second reference for time-sharing the Frequency/Level Counter U6 between the "Frequency-counter" mode and the "A/D Level-measuring" mode. It is also used for the Impulse Noise clock (see paragraph 8-287). When the front panel

"COUNTER" is ON, each one-second cycle is divided as follows: one-half second for frequency-counting, A/D time, and a wait period. The wait period varies with the demand for A/D time. When the front panel "COUNTER" is off, U6 is used exclusively and continuously on A/D level measurements. The Frequency Counter mode is active when U2(19) goes HIGH for one-half second under processor command, during the negative half-cycle of the 1 Hz CLK signal to A60. During this one-half second, U11(9) and U11(4) are HIGH, gating the PLL output from U17(13) into U6 The (L) START line is pulsed LOW immediately after U2(19) goes HIGH and this sets up Latch U18c for the HIGH-to-LOW edge of the 1 Hz clock to start the counter U6. For the "frequency counting" mode, the count must start from zero, therefore the same logic that starts the counter immediately resets it to zero through U12(8) now going HIGH which sets the CLEAR line HIGH at U6(14). At the same time, to ensure a full one-half second time period to count the PLL pulses, the CLEAR lines on all the ÷ 10 Circuits are also set HIGH, and a fresh-starting negative half-cycle of the 1 Hz output now begins. The counter now counts PLL output pulses until the 1 Hz again goes positive (one half-second later) which resets the INHIBIT line HIGH and stops the counter. In this same sequence (H) DONE goes LOW when U6 is counting and HIGH again when the counter stops. This notifies the processor to set U2(19) back to LOW and to read the counter. The counter will contain exactly 10 times the IF frequency in Hertz and .1 Hz resolution is now possible in determining the frequency of the input signal to the instrument. When the count is read out of U6, it is also preset to 990,000. The LSM (Logic State Machine) is now in the idle state and ready for the "A/D Level-Measuring" conversion mode to begin. (See also Section VII (Δ6)).

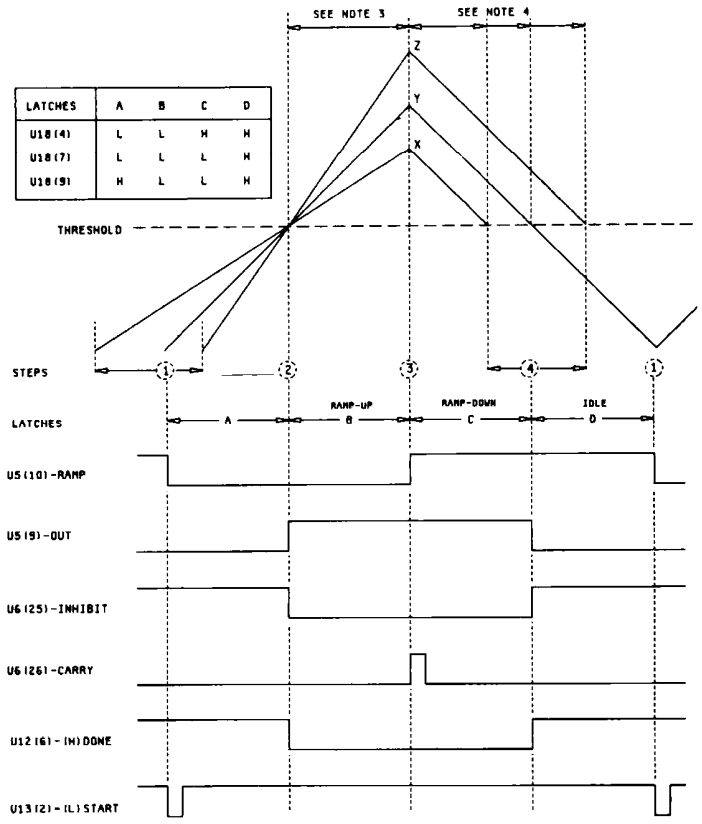
8-174. A/D Conversion. When U2(19) goes LOW during the positive half-cycle of the 1 Hz CLK signal, U11c turns off, U11(5) goes steady HIGH and U11(4) has the 500 kHz output of the ÷ 10 Circuits present as the input for U6. When the front panel COUNTER is OFF, U2(19) will always be LOW placing the counter U6 continuously in the "A/D Level-measuring" mode.

8-175. A/D level-measuring takes place as follows. In the idle state (refer to Figure 8-5) the outputs of latches U18a, b and c are all HIGH. The idle state occurs during the time period between successive A/D conversions. A single A/D conversion takes place in four steps. During each step, the logic state of the output lines of the three U18 latches reflects the step the A/D conversion process is on. In the event of malfunction, if U18 is stable, the cause can be traced (see Figure 8-5).

8-176. Step 1. The processor pulses the (L) START line from HIGH to LOW. The RAMP input (pin 10) of U5 goes LOW, and the A/D Converter begins ramping upwards at a rate determined by the magnitude of the selected input voltage at pins 1 and 2. C7 is charged in one direction as the ramp increases.

8-177. Step 2. When the ramp (voltage on C7) passes an internal threshold of approximately one volt, U5 sets the OUT line (pin 9) from LOW to HIGH. The LSM then removes the HIGH at the INHIBIT (pin 25) of U6 and counter U6 begins counting upwards from a pre-set value of 990,000. The input pulses to the counter come from the 500 kHz output of the ÷ 10 Circuits through U11a and U11b. The LSM also now sets the (H) DONE line to the A60 Controller to LOW.

8-178. Step 3. After 10,000 counts, the counter will contain 1,000,000 and will overflow back to zero. At this time, U6 will set the CARRY line (pin 26) HIGH. The LSM then sets the U5 RAMP back to HIGH and the ramp reverses direction. The ramp now decreases as C7 discharges, but this time at a fixed (calibrated) rate determined by the setting of R21.



NOTES:

1. The ramp-up slope depends on the input voltage to U5 (pins 1 and 2). Z represents a high input and X represents a low input.
2. The ramp height represents the voltage across charging capacitor A22C7.
3. The time between steps (2) and (3) is a fixed time period, determined by the counter going from 990,000 to 1,000,000.
4. The time between steps (3) and (4) varies as a function of how large the input voltage was to U5 and therefore how high the charge on A22C7 became.
5. The ramp-down slope is a constant value for all inputs (set by A22R21).
6. Steps:
   (1) Processor pulses (L) START from HIGH to LOW, forcing "RAMP" from HIGH to LOW. Ramp starts up as A22C7 charges.
   (2) Ramp crosses threshold. U5 sets "OUT" from LOW to HIGH. Counter starts counting from 990,000. "(H) DONE" goes LOW.
   (3) Counter overflows at 1,000,000 from 500kHz pulses and begins counting upwards from zero. U6 pulses "CARRY" from LOW to HIGH, forcing "RAMP" back to HIGH. Ramp starts down as A22C7 discharges at a constant rate.
   (4) Ramp again crosses threshold after time period determined by height of ramp. U5 now sets "OUT" back to LOW. Counter stops. LSM sets "(H) DONE" back to HIGH. Processor now scans U6 for digital number representing value of analog voltage, presetting counter, LSM is idle.

Figure 8-5. A/D Conversion.

8-179. Step 4. The A/D Converter ramps downward until the charge on C7 passes the internal threshold again. At this time, U5 sets the OUT line back to LOW. The LSM now resets the INHIBIT line on U6 to HIGH and the counter stops counting. The LSM also sets the (H) DONE line to HIGH. The processor sees the (H) DONE go HIGH and the sequence of A/D Conversion is complete.

8-180. The count now contained in U6 represents the amplitude of the voltage at the input to U5. the processor now pulses the (H) SCAN line HIGH and after each pulse, samples the output lines of U6 one digit at a time in BCD. The internal circuitry of U6, through U17b, presets the counter to 990,000 as part of the process of reading out the count in U6. After the A/D count is read out and displayed, if the frequency COUNTER is ON, the processor sets U2 pin 19 output to HIGH followed by (L) START to LOW. The LSM is now idle once again and is waiting for the negative half-cycle of the 1 Hz signal to begin frequency counting.

8-181. USB/LSB Oscillators. The third function of the A22 board is unrelated to the other two. The lower sideband (LSB) or upper sideband (USB) oscillator output is sent to the A21 board to mix with the 15.625 kHz second I.F. signal to demodulate the sideband audio. In CAL, with the Impairments option installed (Option 003), a third oscillator signal is switched to the A21 board which comes from the A70 board. That CAL OSC signal, mixed with the second I.F. provides an audio tone back to A70 for weighted filter checks. U101b switches the correct one of the three possible signals to the A21 board by raising two lines HIGH and letting the desired signal pulse through the gate. (L) CAL shuts off both USB and LSB oscillators when LOW to let the CAL OSC signal pass. When CAL is not active, CAL OSC is always HIGH, (L) CAL is HIGH and U2(6) going either HIGH or LOW selects the USB (Y102/Q103 network) or LSB (Y101/Q102 network) oscillator respectively. (See also Section VII (Δ6)).

8-182. The other outputs of U2 control the 8:1 Input Data Selector and pass control lines (H) SMOOTH, (L) 1 MHz ENABLE, and (L) CAL to other boards. U1 accepts the serial control data from the A60 processor and shifts it into a parallel output to U2 which is then latched. U3 selects the output signal to the meter drive amplifier on A21 and U7 selects the input signal to the A/D Converter, both under processor control.

8-183. BBP/OVLD/CAL - A4 (Service Group F).

8-184. The A4 board has three main functions: a broad band power (BBP) level-measuring circuit; an Underload/Overload Detector for input signals, and; the tracking calibration signal generator.

8-185. BBP Level Measuring. The input signal to the instrument is passed through the A2 Input Amplifier board where it is amplified or attenuated (as appropriate) and then passed to the BBP RF input to A4. The function of the BBP detector is to measure the average total broadband (WIDEBAND) power present in the input signal. To accomplish this, the sampling circuits take a representative "slice" or sample of the incoming waveform and the detector measures the power in the sampled signal. The BBP RF signal is amplified +3 dB by Q4 and Q5 (+8 dB in the 3586C) then "sampled" through a diode bridge circuit which is normally biased off.

8-186. The Sampling VCO is frequency-modulated by an 80 Hz oscillator to sweep the range from 20 kHz-50 kHz. This prevents the sampling circuits from performing coherent sampling against any signal in the wideband input. A delay network between U2a and U2b causes the output VCO pulses at T1 to be narrow (25 ns). The pulses from T1 are then used to turn on the diode bridge for a brief period of time to pass a "slice" of the input signal waveform through the +23 dB Amplifier/Driver into the Detector/Logger for amplitude measurement.

8-187. The True RMS Detector Logger determines the overall power level of the sampled input and converts it to a logarithmic DC voltage for use by the A/D Converter A22. The (H) BBA (broadband averaging) line from A2 goes HIGH anytime AVEraging is selected together with WIDEBAND mode. A HIGH on BBA turns on Q8 which shorts out C40 and allows C41 to average the logger "sample" measurements. If AVE is ON when CAL occurs, Q8 is turned off momentarily during the CAL cycle.

8-188. Scaling Amplifier U5B adjusts the Logger output to a scale factor of 100mv/dB in preparation for driving the UL/OL Detector. However, this level is too high to drive the A/D Converter so R34 and R35 divide the signal level by 10 before the signal is passed to the A22 board. Since the BBP LOG RMS signal must pass over the "isolation barrier"

separating the input circuits from the rest of the instrument, the return and the signal lines are resistor-isolated into a balanced input to a buffer amp on A22 which provides common-mode rejection for the DC signal level between the grounds.

8-189. Underload/Overload Detection. The Scaling Amplifier output is passed through a "times 2" amplifier (U5A) to the Underload/Overload Detector. Precision voltage-reference inputs to U6a and U6b set the trip points for the input signal. If either underload or overload occurs, the yellow or red LED's respectively will light, and the UNDERLOAD or OVERLOAD line respectively will go HIGH, notifying the processor on the A60 board that an autorange condition exists. If AUTO Full Scale is selected, the processor will either: (1) increase the overall gain (underload), or (2) attenuate the input signal (overload) by selecting a new FULL SCALE setting. If ENTRY Full Scale is selected, the operator must manually select the correct Full Scale setting. A complete discussion of Range/Full Scale selections is found in the Operating Section of this manual (see paragraph 3-2-66).

8-190. For different front panel modes of operation such as LO NOISE or LO DISTortion, the reference voltage input signal power level in dB that will cause underload or overload to occur can be shifted by 5, 10, or 15 dB as needed (see Table 8-F-1). This is accomplished through processor control of the THRESH 1 and THRESH 2 (threshold) input lines to the Underload/Overload Trip Point Reference circuits. When either of these lines go LOW, current is injected into the node at U5(2), thus controlling input signal power level and effectively shifting the trip points. THRESH 1 going LOW causes a 5 dB change, THRESH 2 LOW causes a 10 dB change and both LOW causes a 15 dB change. For example, if LO DIST mode is selected, THRESH 1 goes LOW, more current is injected into the X2 Amplifier, and the input signal is "raised" in power by a constant 5 dB (effectively lowering the trip points by 5 dB).

8-191. Calibrated Signal Generator. The CAL balanced input to A4 is either the Ø-32.5 MHz tracking oscillator signal originating on the A15 board, or is a fixed 1 MHz signal from the A40 gated through A15. This differential input to A4 is only present in CAL, when the (L) CAL line goes LOW, shutting off Q101 and allowing the bias voltage to be applied to U101a. The Limiter output is sent to a Precision Square Wave Generator which is fed by a Constant Current Source. The current source controls the current flow through the emitters of differential amplifier pair Q102/Q103 by controlling the base voltage of Q104. The (H) LLCAL (low-level cal) line controls whether the CAL OUT signal to A2 is the −40 (low-level) or −20 (high-level) square wave. If −40 out is desired (Full Scale setting of Ø dBm or below), Q106 is turned on and U104a provides no current gain. When −20 out is desired (Full Scale setting of +5 dBm or above), Q106 is off and U104a provides additional gain to increase the power of the CAL OUT signal to A2. The filter components in the generator circuit provide equivalency at the A2 input for the fact that the calibration signal is a square wave where the input signal would normally be a sine wave. Other components provide impedance matching to the A2 input and flatness adjustments for the higher frequencies. The fundamental frequency of the output −40 or −20 signal is at a level such that the true RMS Detector on the IF Gain/Detection board thinks a −40 dBm or −20 dBm signal has been applied to the instrument input. The A4 output differs from −40 dBm or −20 dBm at the input to the A1 board by the insertion loss of A1, and by the fact that the fundamental's level is not equal to the square wave's level.

8-192. Tracking Output - A15 (Service Group F).

8-193. The A15 board accepts the 50-82.5 MHz first L.O. signal from A51, beats it against the 50 MHz instrument Frequency Reference output from A40, and produces a 0-32.5 MHz

output signal which tracks the front panel tuned-frequency. This output signal is available at the rear panel BNC connector (J5) labeled Fo (0-32 MHz) and is also sent to the A4 board to be used as the tracking CAL signal whenever CAL is active. The rear panel BNC output is maintained at approximately Ø dBm by a leveling loop which controls the amplitude of the 50 MHz input to the mixer.

8-194. The 50-82.5 MHz first L.O. input to the double-balanced mixer is amplified and limited inside U1 so that any amplitude changes that occur with frequency are not noticed in the output of the mixer. The 50 MHz input of U1, however, is a linear port, i.e., a 2 dB change in input signal amplitude will be seen as a 2 dB change in the mixer output. Therefore, a variable voltage applied through R8 to the 50 MHz input can provide level control feed back.

8-195. The Ø-32.5 MHz output from U1 is amplified by U2 and goes two directions. One output feeds a Power Amplifier stage that drives the rear panel tracking output J5. In the event this output is erroneously connected to a source, overload protection circuitry is provided. At the Power Amplifier output, a signal tap is provided to a Peak-to-Peak Level Detector that, together with integrator U3, maintains Ø dB (±0.5 dB) at the rear panel J5 output using voltage-control feedback to U1.

8-196. The other output of U2 goes into a buffer circuit (U4) which also squares the signal at ECL levels for input to ECL gate U5. The (L) CAL line turns Q4 off when in CAL which allows U4 to pass the CAL SIGNAL to U5d. A second input to U5d is a buffered 1 MHz from A40. When internal self-test TF12 (paragraph 8-79) is selected, the (L) 1 MHz ENABLE line goes LOW simultaneously with (L) CAL going HIGH. This shuts off U4 (Ø-32.5 MHz) and turns on U5a, b and c, passing the 1 MHz signal through U5d to the A4 board.

8-197. First Local Oscillator - (Service Groups D and E).

8-198. The first L.O. signal (50-82.5 MHz) in the 3586A/B/C is generated by seven separate P.C. boards comprising three separate loops: Step, Sum and Fractional-N. Refer to Figure 8-6. The Step Loop (A50) locks up under processor control to 54-86MHz in exactly 2MHz steps depending on the desired L.O. frequency. The step frequency is mixed with the present L.O. frequency (50-82.5 MHz) in the Sum Loop Mixer (A52) to produce a difference frequency between 2 MHz and 4 MHz which is one input to the Sum Loop Phase Detector (A53). The other input is a 2-4 MHz reference signal from the Fractional-N Loop. The Fractional-N VCO (A31) locks up under processor control to a precise frequency, with 1 Hz resolution, between 20 MHz and 40 MHz. This frequency is then divided-by-ten to produce a 2-4 MHz reference input to the Sum Loop Phase Detector that has 0.1 Hz resolution. The phase difference between the two 2-4 MHz inputs produces a DC tuning voltage which changes the frequency of the Sum Loop VCO (A51) to the exact desired L.O. frequency in the range 50-82.5 MHz. The Step tuning voltage, besides tuning the Step Loop VCO, is fed to a voltage comparator in the Summing circuits as a reference for the Sum tuning voltage. This provides the coarse frequency stepping of the Sum Loop VCO while the Fractional-N Loop provides the fine frequency control. The Sum Loop VCO output (50-82.5 MHz) has the exact same frequency resolution and stability as the 2-4 MHz from the Fractional-N VCO.

8-199. Step Loop - A50 (Service Group D).

8-200. The Step Loop is fully contained on the A50 board and consists of the four basic elements of a phase-locked-loop (PLL): a voltage-controlled oscillator (VCO), a divide-by-N circuit (÷N), a phase detector, and a low-pass filter (LPF).

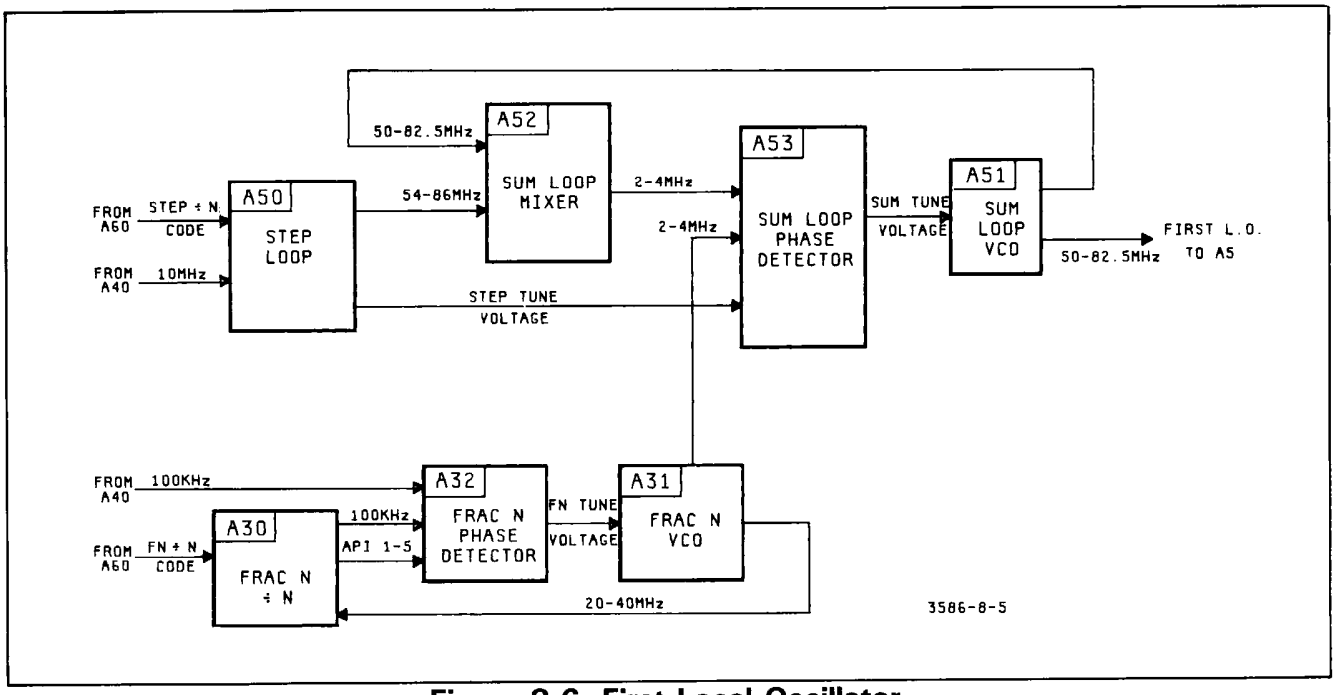


Figure 8-6. First Local Oscillator.

8-201. Step Loop VCO. The VCO operates in the range of 54-86 MHz in 2 MHz steps. The actual frequency is controlled by the STEP TUNE VOLTAGE across the voltage-variable-capacitance (VARICAP) diodes CR1 and CR2. The STEP TUNE voltage can vary from +9 VDC to −9 VDC, changing the capacitance of the VARICAPS and thus changing the frequency of the oscillator.

8-202. The VCO output is buffered by Q7 and Q8 and then goes two directions. One path goes to two isolation amplifiers which provide a test jack capability for monitoring the Step VCO frequency (J2) and an output to the Sum Loop Mixer (A52). The other path is through an isolation amplifier to an ECL Waveshaper which converts the sine wave to a square wave output at ECL levels to drive the ÷N circuit.

8-203. Step Loop Divide-By-N. A programmable ÷N counter is used to divide the present VCO frequency down to 2 MHz for the variable input to the phase detector. The processor sends a ÷N code (where N is an integer from 27 to 43) over lines F1, F2, F4, F8, F10, and F20 to counters U71 and U72. The counters accept the VCO input, count the pulses, divide the count by the selected integer and output the result to the phase detector. When the Step Loop is "locked", the divider output frequency is 2 MHz.

8-204. Step Loop Phase Detector. The phase detector has two inputs. The first input comes into A50 as a 10 MHz reference from the A40 board. A Divider/Waveshaper converts this 10 MHz pulse to a 2 MHz pulse as the precision reference input to the phase detector. The second input is from the ÷N circuit which varies about 2 MHz as a function of the present VCO frequency and the processor-selected value of N.

8-205. The phase detector compares the 2 MHz variable input from the ÷N to the fixed 2 MHz precision reference. If the rising edges of the pulses are at the proper phase, the VCO has the correct frequency ordered by the processor, the loop is phase-locked and the STEP TUNE DC voltage across main-loop charging capacitor C48 is constant, holding the VCO

frequency constant. The positive and Negative Current Sources are now exactly in phase, and no current flows through S1 and R50 into C48.

8-206. If the VCO frequency is too low (Example: operator changes frequency upwards, processor increases N, ÷N output is less than 2 MHz), the variable input pulse now lags the reference input pulse. The Negative Current Source (Q71) will now be turned on longer than the Positive Current Source (Q72) and the voltage across C48 will decrease as current flows through R50 and S1 into Q71. As the voltage across C48 goes more negative than it was, the VCO will increase in frequency until the variable input is again in phase with the reference. Now the Negative and Positive Current sources will again turn on and off together at the 2 MHz rate set by the reference input, no more current flows and the loop is again locked. For a VCO frequency too high the circuit action is reversed. The Positive Source is on longer than the Negative, current flows out of Q72 into C48 and the VCO frequency decreases until the loop is again locked.

8-207. The switching amplifiers have differential, simultaneous, out-of-phase inputs to ensure quick turn-on and turn-off of the two current sources. The TEST position of S1 taps a fixed reference voltage for VCO frequency adjustment and test.

8-208. Step Loop Low Pass Filter. The LPF keeps the 2 MHz pulses of current flow from adding 2 MHz sidebands to the VCO output. The output of the LPF also goes to a unity gain Buffer stage (U1) and then on to the STEP/SUM Voltage Comparator on the A53 board.

8-209. U1 feeds an Unlock Detector circuit (U73) which compares the STEP TUNE voltage to ±9V. If the loop is not locked up (or is locked up at too high or low a frequency), the STEP TUNE voltage will exceed the UNLOCK thresholds, DS70 will turn on and the processor will be notified via a LOW on (L) STEP UNLOCK to present error code E3.8 (Step Loop unlocked) in the MEASUREMENT/ENTRY display area.

8-210. Sum Loop - A51, A52, A53 (Service Group D).

8-211. The Sum Loop is composed of three P.C. boards. It is a phase-locked loop in which a mixer circuit replaces the standard divide-by-N circuit, the reference input to the phase detector is programmable by the processor, and some comparator circuits and switching logic help the loop handle large frequency changes by the operator.

8-212. Sum Loop VCO (A51). The VCO operates in the frequency range of 50-82.5 MHz in 0.1 Hz steps. The actual frequency is controlled by the SUM TUNING VOLTAGE which is felt across VARICAP diodes CR1 and CR2. (It is important that both STEP and SUM loops track together very closely, therefore A50CR1, A50CR2, A51CR1 and A51CR2 are a four-component matched set. If one VARICAP must be replaced, all four must be replaced.) S1 provides a fixed voltage tap in the TEST position for VCO frequency adjustment and test.

8-213. The VCO output is buffered by Q11 and then uses two emitter-followers to drive the four outputs through the isolation amplifiers. The 100 MHz LPF's provide rejection of harmonics.

8-214. Sum Loop Mixer (A52). The mixer stage has two inputs, the 54-86 MHz output from the Step Loop VCO and the 50-82.5 MHz output of the Sum Loop VCO. These two signals are mixed together to provide a difference frequency between 2 MHz and 4 MHz.

8-215. The mixer output is amplified and filtered to remove high-frequency components

and then drives a wave-shaper circuit. The output of Q2 is a sine-wave which U2 converts to a square-wave at an ECL output level to drive the Sum Loop Phase Detector A53.

8-216. Sum Loop Phase Detector (A53). The 2-4 MHz variable input from the Sum mixer (A52) is limited by U7 at an ECL input level to U6b. The 2-4 MHz reference input from the Fractional-N Loop is phase-compared to the variable input, and Positive/Negative current sources are then turned on and off as necessary to change the SUM TUNING VOLTAGE to the Sum VCO.

8-217. When the Sum Loop is phase-locked to the Fractional-N reference, the outputs of the current sources (Q4 and Q5) are exactly in sync, so no current flows through the Low Pass Filter either to or from the Sum Loop VCO and the Sum VCO frequency is stable. If the operator makes a front panel frequency change so that only the Franctional-N reference is changed, the loop will momentarily unlock. The phase detector will then adjust the on/off time duration of the appropriate current source to raise or lower the SUM TUNING VOLTAGE. The SUM TUNING VOLTAGE is sent to the Sum VCO (A51). The Sum VCO frequency will change accordingly, the A52 mixer output will follow the VCO change and, when it equals the Fractional-N reference, the loop will again stabilize.

8-218. If a frequency change is made from the front panel the processor will first re-program the Fractional-N loop and then, if necessary change the Step loop frequency. If the Step VCO frequency change causes the A52 Mixer output to be greater than approximately 10 MHz, the A52 LPF will not pass the signal, the Sum Mixer input to the phase detector will die and the Sum Loop would try to drive to one end as commanded by the Sum Phase Detector. However, the STEP TUNING VOLTAGE changes with the Step Loop and this voltage is input to Differential Amplifier A53U1. U1 drives the Loop Synchronization Comparator circuit to handle these "loop-out-of-limit" conditions. The output of either U3a or U3b will now change state, as required, to over-ride the phase detector and drive the Sum Loop VCO up or down in frequency until the loop is back within limits. At this time, the Fractional-N reference will again assume control of the loop until phase-lock occurs.

8-219. In normal (locked loop) operation, the output of U1 is approximately Ø volts, the output of U3a is HIGH and the output of U3b is LOW. If the loop unlocks with the Sum VCO too low and out of limits, the STEP TUNING voltage will be instantaneously more negative than the SUM TUNING voltage. U1 output now goes positive causing U3a output to go LOW. This state change of U3a turns the Negative current source on. It also freezes the Phase Detector flip-flops by putting a LOW on the D inputs of U6a and U6b. This turns the Positive Current source off to pull the Sum VCO frequency up to within 2 MHz of the Step VCO. When the SUM TUNING VOLTAGE lowers at the input of U1 sufficiently to return U1 output to Ø volts, U3a reverses state, the loop is within operating limits and the Phase Detector again assumes control and locks up the loop. During this sequence, the output of U3b would remain constant.

8-220. If the loop unlocks with the Sum VCO too high and out of limits, the process is similar but the Negative current source turns off (U3b changes state) and the Positive source turns on until the Sum VCO comes down to within 2 MHz of the Step VCO. When the Phase Detector assumes control, it again locks up the Sum Loop to agree with the Fractional-N loop.

8-221. Anytime the Sum Loop goes to an "out-of-limit" condition, one of the two inputs to U4a will go HIGH turning Q1 on to light the unlock indicator DS1. At the same time, this LOW at pin 2 of U4a is sent to the processor via the SUM UNLOCK (L) line to cause the E 3.2 error code (Sum loop unlocked) to be displayed.

8-222. Fractional-N Loop - A30, A31, A32 (Service Group E).

8-223. The Fractional-N (FN) circuits form a phase-locked loop that operates at a selected frequency between 20 MHz and 40 MHz under processor control. Refer to Figure 8-6. The FN VCO frequency is passed through a divide-by-ten circuit and the resulting 2 MHz to 4 MHz signal, with 0.1 Hz resolution, becomes the variable reference input to the Sum loop phase detector. The FN logic circuits provide precise control of the FN VCO to obtain the exact desired frequency with 1 Hz resolution. The ÷ 10 circuit then provides 0.1 Hz resolution. Three PC boards contain the FN circuitry: A31 (FN VCO), A32 (FN Phase Detector), A30 (FN ÷N).

8-224. Fractional-N VCO (A31). The A31 FN VCO receives a DC voltage (FN TUNE) from the FN phase detector A32. The tuning voltage (Ø to +6 volts) is passed through a variable gain amplifier (U1a) and then is applied to CR4, CR5, and CR6 to set the VCO at a frequency between 20 MHz (+6 volts) and 40 MHz (Ø volts). A stable cathode bias for the VARICAP's is provided by U1b through tank coil L4. The VCO output is buffered by Q3 and Q4 and then takes three separate paths. One path is through Q5 and Q6 to the A30 board (FN ÷N). A second path provides a test jack, (TP1) on A31 for monitoring the 20-40 MHz VCO frequency. The third path (through Q7 and Q8) is to a waveshaper circuit which converts the VCO sine wave to an ECL square wave to drive the ÷ 10 circuit (U3). U3 provides two separate 2-4 MHz outputs, one to TP2 and the other a buffered variable-reference input to the Sum Loop phase detector A53.

8-225. The FN TUNE voltage is also applied to a dual comparator (U2a and U2b) to detect whether an "out-of-lock" condition exists. If the tuning voltage is greater than +8.6 volts or less than −8.6 volts, U2a or U2b respectively will turn Q9 on. When Q9 turns on, LED CR11 will illuminate and the (L) FN UNLOCK line will go LOW, telling the processor to display error code E 3.4 (FN loop unlocked).

8-226. Fractional-N Phase Detector (A32). The A32 FN Phase Detector compares the phase relationship of a frequency-variable 100 kHz signal from the FN ÷N A30 board to a stable 100 kHz reference signal from the A40 board. A negative-going pulse is then generated, whose width is the time between leading edges of the two input signal pulses to U1. This pulse controls the ramp-up time of an integrator circuit to generate the control voltage for the FN VCO. The ramp-down time of the integrator, in between reference pulses, is initiated by the turn-on of a fixed Bias current that is modified by five control currents. These currents perform a function called Analog Phase Interpolation (API). The current sources and associated switches are called API's. The on/off signals for the control currents come from a Fractional-N chip on the A30 board and are labeled API-1 through API-5. Control of these five currents enables the precision tuning of the FN VCO in 1 Hertz increments. A Sample/Hold circuit keeps the changing integrator output from modulating the FN TUNE voltage. When the ramp-up is complete, the voltage on the integrator is sampled and then passed to the FN VCO. See Figure 8-7 for a graphic representation of the output voltage from the integrator.

8-227. The 100 kHz input pulse from the FN ÷N normally arrives at U1 before the reference input pulse. The outputs of U1a are switched by this pulse through Q1 and Q2 to turn Q3 off and Q4 on. TP8 now goes LOW, turning CR3 off and starting the "ramp-up" time of the integrator. When the 100 kHz reference pulse arrives at U1b, U1a is reset, Q1 and Q2 are switched again, Q3 turns on and Q4 turns off. TP8 now goes HIGH, CR3 turns on and ramp-up stops. The integrator now has a constant output as shown by the flat portion (A) in Figure 8-7 and this level is sampled and passed to the FN VCO. U1b will be reset by the next pulse from A30.

8-228. When the BIAS line goes HIGH at U3(14) and the LATCH CLOCK triggers U3, the "ramp down" time begins. The first part of the ramp-down current shown (B) in Figure 8-7 is Bias current only applied to the integrator. All ramp-down current flows into U5. The LATCH CLOCK is now triggering U3 at the rate FN VCO ÷ 10, called "API Clock". At all times other than during ramp-down, LATCH CLOCK is held HIGH by the LOW present on the BIAS line (on the A30 board). After several API Clock pulses, a pre-determined (see FN ÷ N discussion in paragraph 8-233) combination of API lines 1 to 5 are switched to modify the Bias current with API current as shown at (C) in Figure 8-7. The selected API current-sinks absorb a precise amount of the Bias current so that the slope of the integrator ramp-down is decreased. Each API current-sink absorbs 10 times more current than the one next to it with API-1 absorbing the most and API-5 the least. These current sinks are turned on and off by the outputs of U3 and Q18-Q20. This API-current cycle lasts for 10 pulses of the API Clock. Each current-sink may be on for 0-9 of the 10 pulses so that any numerical combination from 0 to 99,999 is possible.

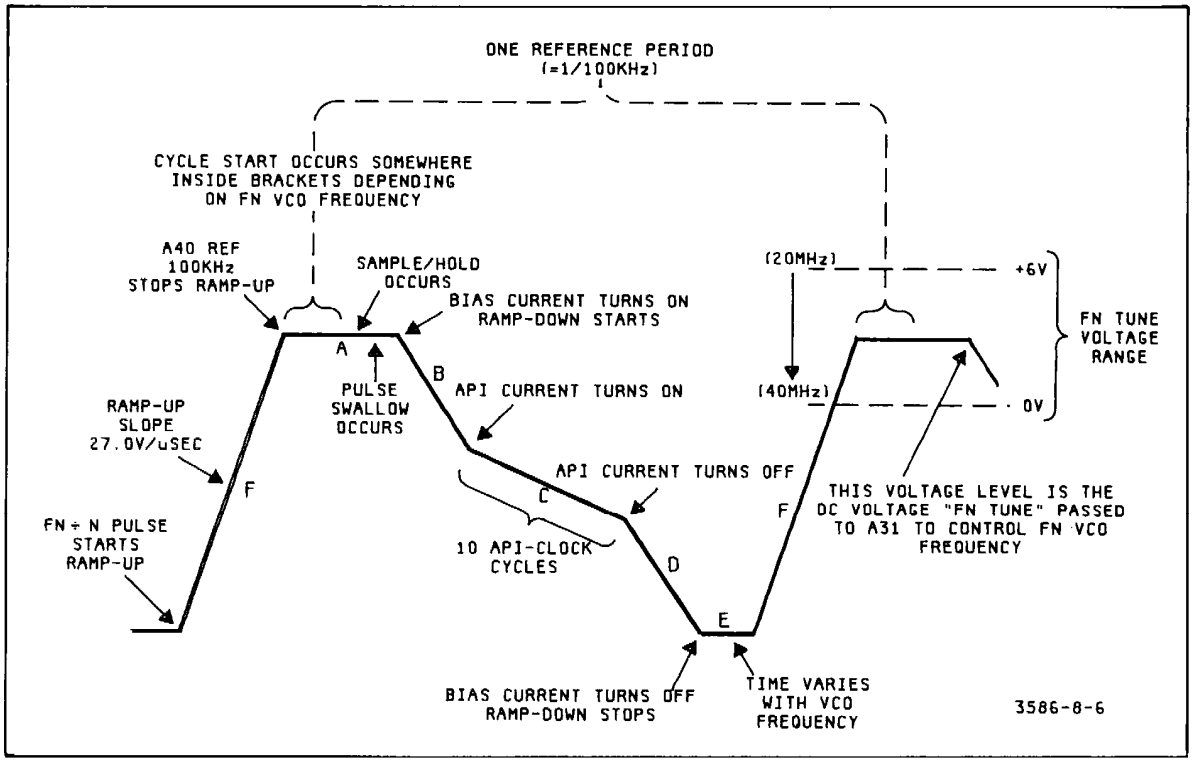


Figure 8-7. Fractional-N Integrator Output (A32TP2).

8-229. Next the API current-sinks are switched out of the integrator loop and again only the Bias current ramps the Integrator downward (D). When the Bias current is turned off after a specific number of API clock (FN VCO ÷ 10) pulses, the integrator is momentarily in a quiescent state (E). This rest state varies in time depending on VCO frequency but it ends upon receipt of the next FN ÷ N 100 kHz pulse at the phase detector. This pulse again begins "ramp-up" (F) and at the receipt of the 100 kHz reference pulse which stops ramp-up, the reference period is complete. The duration of the ramp-down time is controlled by the Fractional-N chip on A30.

8-230. Sample and Hold occurs during the (A) portion of the integrator waveform. Shortly after the 100 kHz reference pulse shuts off the ramp-up, the FN Logic chip on A30 sets the S + H line HIGH. Q80 provides buffering, Q81 shifts the level, and open-collector switches U8a-U8d now bias and turn on Q32 and Q33. C11 charges to (samples) a DC level equal to

the integrator "top-of-the-ramp" output voltage; the S + H line now goes LOW and C11 "holds" the FN TUNE voltage for the FN VCO.

8-231. Bias constant-current source Q21 feeds into the +5 volt node at the input to the BIAS/API Current Summation Amplifier. Q8, Q10 and Q11 hold this node at a constant +5 volts, permitting precise current division in the five API lines. The API current-sinks then siphon off current from that node to control the slope of the integrator ramp-down.

8-232. The integrator input at the gate of Q22a is held at virtual ground (Ø volts D.C.) by grounding the gate of Q22b. Q22 provides a high impedance input stage with unity gain. Q24,Q25,Q26 and Q27 form a high-gain, high speed operational amplifier to satisfy the ramp-up, ramp-down speed requirements of the integrator. Q28, Q29, Q30 and Q31 provide a very low impedance output with low-distortion for ramp-up current output.

8-233. Fractional-N ÷ N (A30). The A30 board provides the ÷ N function for the FN phase-locked loop. The heart of this operation is the Fractional-N Logic chip U16 which receives instructions and data from the processor on the A60 Controller board.

8-234. 3586 Fractional-N Logic controls the FN VCO in the FN phase-locked loop at a frequency which will yield the exact desired tuned frequency while using a whole integer as the FN loop ÷N number. For example, if a front panel frequency of 3.603 MHz is desired, the processor adds this frequency to 54 MHz and divides by two to determine the ÷N number for the Step Loop (in this case, 28). The remainder (1.603) is subtracted from 4 MHz to obtain 2.397 MHz as the desired frequency input to the A53 Sum Loop Phase Detector from the FN loop. To obtain this frequency out of the A31 FN VCO ÷10 circuit, the FN VCO must run ten times higher at 23.97 MHz. The processor sends the frequency command to the FN Logic chip U16 which determines the whole integer ÷N number for the XXX to 999 counter and the fractional portion of the frequency for "pulse-swallow" determination and for API current calculation. For this example, the ÷N number is 239 and the fractional number is .7. U16 sends the 9's complement of the ÷N number (999-239 = 760) to preset the XXX to 999 counter to 760. When the counter increments from 760 to 999 as clocked by the FN VCO frequency, the next clock pulse causes the counter to roll over and generate a "Cycle Start" pulse that begins a new reference period. This roll-over occurs at a 100 kHz rate which is also the variable frequency input to the A32 FN Phase Detector (23,900,000 Hz ÷ 239 = 100,000 Hz). Note that the input to the counter must be 23,900,000 Hz even though the FN VCO is running at 23,970,000 Hz. The fractional number .7, saved by U16, is used to determine when to "swallow" one of the FN VCO pulses entering the Pulse Delete Gate (U4c) so that the average frequency of the signal going into the counter is an exact 100 kHz multiple of the ÷N number. The .7 is also used to calculate the needed amount of API Current during "ramp-down" of the A32 Integrator.

8-235. All FN operations are defined in terms of a reference period which covers a complete cycle of the output of the Integrator circuit on the A32 board. At the beginning of a new reference period, the XXX to 999 counter rolls over at 999 to generate the "cycle-start" pulse to U16 for the new period. U16 now controls the following FN operations.

1. The Integrator output is sampled and passed to the FN VCO.

2. If 360° or more of phase accumulation has occurred within U16 during the previous reference period, a "pulse-swallow" occurs at the FN VCO input to the ÷N counter.

3. The positive Bias current is switched into the integrator.

4. The negative API current sources are switched into the integator, siphoning out a calculated amount of Bias current.

5. The API current sources are switched off, followed by the Bias current source.

6. Output data is sent to the counter in 9's complement to preset the ÷N number for the next reference period. This is done during the last six counts (993-999) of the counter.

8-236. When the Bias current is switched off, U16(10) goes LOW, reversing the inputs to U11b and therefore to U12a. Before the counter rolls over, a clock pulse (FN VCO ÷ 2) triggers U12a, Q1 turns on at the next FN VCO clock pulse to U12b, TP3 goes HIGH and a new 100 kHz variable frequency input pulse is sent to the phase detector to begin "ramp-up". After a short time period, which is dependent upon the FN VCO frequency, the counter rolls over, a new "cycle start" pulse is generated and a new reference period begins. After the "cycle start" pulse is received, U16 sets the S + H line (pin 11) to HIGH to sample the integrator output and then LOW to hold the FN TUNE voltage for the FN VCO. Circuit timing, by design, ensures that the Sample/Hold operation does not occur until ramp-up is complete.

8-237. Some discussion of pulse-swallow theory is helpful at this point to understand FN operation. If there were no pulse swallow, a phase-locked loop VCO would run at an exact multiple N of the reference input to the Phase Detector "in-phase" with the reference input, the loop would be locked and the VCO output would be constant. This kind of loop, however, has limited applications. When small frequency increments are desired, the ÷N counter range must become very large, an expensive and complex design procedure. Fractional-N logic, using a "pulse-swallow" technique is a satisfactory solution to this problem.

8-238. If we were to open the tuning voltage line to the VCO and, using some precision DC voltage source, increment the VCO frequency by 1 Hz, the variable input to the Phase Detector (VCO ÷N) would be slightly higher in frequency than the reference input and therefore would lead in phase by a fixed number of degrees after one reference period. If this situation was not corrected, the phase error would accumulate with each input pulse until 360° of phase error at the VCO frequency existed, at which time the inputs would again be in-phase.

8-239. Since the phase error is predictable for any change in VCO frequency, we can calculate how long it will take for 360° of phase error to occur for any frequency difference between the VCO ÷N input and the reference input. When 360° of phase error is accumulated, if we then stop one pulse of the VCO output from entering the ÷N counter, the average number of pulses entering the counter (divided-by-N, in the counter) will produce a variable input at the Phase Detector which will be in-phase with the reference input. This occurs even though the VCO is operating at a frequency that is a fractional number multiple of the reference while N is an integer. In the 3586, the above logical operations, where a VCO pulse is "swallowed" before it can enter the ÷N counter, are controlled by the FN Logic chip U16.

8-240. After the sample/hold operation takes place, the FN Logic chip U16 determines if 360° or more of phase error has accumulated since the last pulse-swallow. If yes, the PS line, U16(12), to U14(2) is set momentarily HIGH and this signal is gated through to Pulse Delete Gate U4c where it shows up as a one-shot LOW pulse that inhibits one pulse of the VCO input to the counter.

8-241. After the PS line again goes LOW, the BIAS line is set HIGH to the integrator on A32 and ramp-down begins. After several pulses of the Chip Clock (VCO ÷ 10), a precisely-controlled amount of API current is turned on at the A32 board by U16 control of lines API-1 to API-5. If the desired frequency is not an exact multiple of .1 MHz, API current will be flowing during each reference period. When a change in frequency is ordered by the processor, U16 calculates the amount of API-current required to modify the ramp-down slope of the Integrator. Then, after the Bias current is turned on, one or more of the five API current sinks on A32 are turned on for up to 9 pulses of the Chip Clock for each control line. This whole operation causes the integrator output to ramp up or down to a new level of FN TUNE voltage, thereby changing the FN VCO to the new frequency. Because very precise control of API current is possible, very small incremental frequency changes are possible. Since the 3586 has .1 Hz resolution, the FN VCO is controlled in 1 Hz steps so that the FN VCO ÷ 10 output will step in .1 Hz increments.

8-242. After ten API-Clock pulses, all API control lines are turned off, followed a few clock pulses later by the BIAS line going LOW which turns off the Bias current and ramp-down ceases. After a short period of time, determined by the current frequency setting and therefore by the ÷ N number, the counter rolls over, a new "Cycle-Start" pulse is generated and a new reference period begins.

8-243. For a given frequency change, U16 determines the new ÷ N number which could range from 200 to 400 since the FN VCO can operate from 20 MHz to 40 MHz. If for example, the desired instrument frequency is 18,450,330.3 Hz, the processor adds 54 MHz to the number of MHz in the desired frequency (18) to obtain the Step VCO frequency (72 MHz). It then divides by two to obtain the Step loop ÷ N number(36) which it sends to A50. The remainder (450,330.3 Hz) is subtracted from 4 MHz and sent to the FN Logic chip U16 (4,000,000.0-450,330.3 = 3,549,669.7). This is the desired reference input to the Sum Loop Phase Detector. The FN Logic chip breaks this frequency into two components without regard to the decimal place (354 = ÷ N number, 96697 = API line programming). The 354 is subtracted from 999 (= 645) and sent to preset the counter. The 96697 is used to control API 1 to API 5 turn-on times (API 1 is turned on for 9 of the 10 API-Clock pulses, API 2 for 6 pulses, etc.) The FN loop is calibrated so that the resulting FN TUNE integrator output voltage will exactly tune the FN VCO to 35,496,697 Hz, and the desired frequency for the input to the Sum Loop phase detector (FN VCO ÷ 10 = 3,549,669.7 Hz) is obtained. The Sum Loop tuning voltage will now drive the Sum VCO to 68,450,330.3 Hz which will beat with the Step VCO frequency of 72,000,000.0 Hz in the Sum Loop Mixer to also obtain 3,549,669.7 Hz as the other input to the phase detector. The Sum VCO output is also the First L.O. frequency and when it beats with the input signal to the instrument of 18,450,330.3 Hz, the first I.F. of 50 MHz is derived out of the First Mixer A5.

8-244. Second Local Oscillator - A11 (Service Group B).

8-245. The Second L.O. has a frequency which is exactly 49.984375 MHz and which is mixed with the first I.F. (50 MHz) in the Second Mixer (A10) to produce the second I.F. of 15.625 kHz. This very stable frequency is obtained by fine tuning a voltage-controlled crystal oscillator (VCXO) that uses a 49.9843 MHz crystal in the feedback circuit. The VCXO is one component of a phase-locked loop (PLL) that uses the same Frequency Reference (A40) as the first L.O. for phase stability and frequency accuracy.

8-246. The VCXO output of 49.984375 MHz takes two paths, one to the Second Mixer board A10 through buffer U44 and the other to the PLL mixer U50 through buffer U33. The second input to U50 is the 50 MHz frequency reference from the A40 Board. These two

signals mixed together furnish the 15.625 kHz variable input to Phase Detector U70b through Waveshaper U60.

8-247. The reference input to the Phase Detector comes from the A40 board as a 1 MHz low-level signal, is shaped by Q10 and Q11 to a TTL square wave and input to U70a. The "a" half of U70 is a selectable "divide-by" circuit which is hard-wired for ÷64. The I MHz square wave from Q10/11, divided by 64 in U70a gives the stable 15.625 kHz reference input internally to Phase Detector U70b. The variable 15.625 kHz input from mixer U50 is compared in U70b to the reference input and a DC tuning voltage is generated and passed to U80. Integrator U80 filters out the frequency components present on the tuning voltage so that TP2 is a DC level to be passed to the VCXO.

8-248. U90 is a dual comparator used to detect a "loop-unlocked" condition. If the loop starts to drift, U80 will drive it quickly to the positive or negative rail and as soon as the voltage at U90(3,6) exceeds ±10.5 VDC,, one of the open-collector outputs of U90 will go LOW. CR91 will then turn on and the (L) 2nd L.O. UNLOCK line notifies the A60 processor to display error code E 3.1 (Second L.O. unlocked) on the front panel of the instrument.

8-249. Controller - A60 (Service Group C).

8-250. All digital operations inside the 3586A/B/C are managed by the micro-processor on the A60 Controller together with its associated software stored in six ROM's. In addition, two NMOS and two CMOS RAM's provide "scratch pad" memory and data storage capabilities. The processor handles all front panel switch depressions, changes instrument measurement modes, processes data, commands display changes, monitors P.C. board status, performs automatic calibration and, upon command, initiates internal self-test procedures.

8-251. Microprocessor U6 has three types of input/output. There are: 16 address lines (AØ-A15) for selecting a particular ROM or RAM memory address; 8 data lines (DØ-D7) for reading data or instructions into the processor from ROM or RAM memory or for writing data into a RAM memory address; 9 control lines for directing read/write operation, timing signals, enable, interrupt and reset operations. Seven of the address lines, AØ-A2 and A12-A15, are also used to select one of eight different combinations of input data from various circuits in the instrument, each combination then being passed to the processor over the 8 data lines. The processor can also send output data to different circuits via the 8 data lines to U18, the Parallel Interface Adapter (PIA). The PIA directs the output data to the correct circuit over one of its two data buses, Port A or Port B. All Mnemonics on A60 control lines use positive logic. For example, R/$\overline{W}$ means that, when this line is HIGH, the processor is performing a Read operation. When LOW, a Write operation is in process.

8-252. Microprocessor Operation. Timing for the processor is furnished by Clock Generator U5. A 3.8 MHz oscillator circuit provides the basic timing frequency to U5. U5 then provides outputs at that frequency (4xfo), half that frequency (2xfo), and one-fourth that frequency (ϕ1 and ϕ2) to control all processor operations. A start-up circuit keeps the processor from running until the +5v supply voltage is stabilized. It does this by holding the $\overline{\text{RESET}}$ line to U6 in a LOW state until C1 charges up sufficiently to let the $\overline{\text{RESET}}$ line go HIGH. Comparator U23 also monitors the +5v supply for ripple or noise spikes. One side of the comparator input is heavily filtered and the other side is not. A sharp, narrow spike on the +5v will not cause a system reset because C21 and C29 will filter it out, but C21 is not large enough to handle wider spikes or AC ripple like C29 can. Therefore, the

comparator will trip on either of these conditions, C30 will give positive feedback to speed the comparator output in going LOW and C1 will discharge through CR7 into U23. When the transient is gone or C30 is completely charged, the comparator will flip back, C1 will again charge and the HIGH on the $\overline{\text{SYSTEM RESET}}$ of U5 will force the $\overline{\text{RESET}}$ line HIGH to U6 to re-start the processor. S1(1) provides a manual means of resetting the processor by shorting out C1. U23 will not detect excessively high or low steady-state conditions of the +5v supply.

8-253. U2a, U3, U4b and U4d provide gating for the Write Enable Line ($\overline{\text{WE}}$) to ensure data is properly written into the NMOS RAM's U14 and U16.

8-254. Memory Operation (ROM/RAM). As clocked by the ϕ1 and ϕ2 inputs from U5, processor U6 performs fetch and execute operations from ROM memory. During the fetch phase, U6 places a word on bits AØ-A11 of the address bus which is sent in parallel to all six of the ROM's (U7-U12). At the same time, a three-bit select code is placed on bits A12-A14 to ROM-Select chip U24. The select code determines which one of the ROM's is the desired one and it enables only that ROM to output data on the data lines. The selected ROM places its data on lines DØ to D7 which are buffered by U13 and then input to U6 via the data bus and stored internally in U6. U13 is gated by U2b when bit A15 is set HIGH and the Read/$\overline{\text{Write}}$ line (R/$\overline{\text{W}}$) is set High ("Read from ROM" condition) and ϕ2 is also HIGH. During the execute phase, U6 examines the instruction word from ROM and carries out the instruction.

8-255. RAM memory shares the same address bus with ROM memory. When A15 is set LOW, a "Read from RAM" condition exists and U26 is used to decode bits A12-A14 and select the proper RAM pair for a read operation. For "Read from RAM", U2a is off because R/$\overline{\text{W}}$ is HIGH and therefore the Write Enable line ($\overline{\text{WE}}$) to U14 and U16 is HIGH and the R/$\overline{\text{W}}$ line to U28 and U29 is also HIGH. Bits AØ and A9 now select the desired address for NMOS RAM (bits AØ to A7 for CMOS RAM) and a single 8 bit data word is assembled from the selected RAM pair (U14/U16 or U28/U29) and passed through shorting network J1 (provided for troubleshooting procedures) to the processor data bus.

8-256. The NMOS RAM pair (U14/U16) is used for normal operations of the instrument. The CMOS RAM pair (U28/U29) is used only to perform the STORE/RECALL operations from the front panel, where up to nine different front panel mode/frequency configurations may be stored and recalled by the operator. A nickel-cadmium battery, which is physically located on the A80 board, provides a "keep-alive" voltage (V-BAT) to the CMOS RAM's so that these stored configurations are retained even with the instrument turned off for extended periods. The select line from U26(14) to CMOS RAM has a filter network composed of R26, R27, and C37 which protects the CMOS chips from transients at instrument turn-on. Additional protection for the CMOS data is provided by Q1 and other components which keep transients from disturbing the stored data on U28 and U29. Writing into RAM memory occurs when the respective RAM write enable lines, U28/U29(16) and U14/U16(10), are set LOW. The processor puts the address to be written into on the address bus and then puts the word destined for that address on the data bus.

8-257. U26 also controls the selection of input/output (I/O) data to or from other circuits in the instrument. When R/$\overline{\text{W}}$ is HIGH and U26 selects $\overline{\text{Y6}}$ (pin 9) LOW, U25(6) output goes LOW and S will strobe input data onto the data bus from the Input Multiplexers. When R/$\overline{\text{W}}$ is LOW and U26 selects $\overline{\text{Y4}}$ (pin 11) LOW, $\overline{\text{CS2}}$ selects U18 (PIA) to accept data from the processor and output it from Port A or Port B as determined by address lines AØ and A1 into U18. Address line A11 HIGH, in conjunction with $\overline{\text{CS2}}$ LOW enables the PIA. Line E clocks the data transfer.

8-258. Input/Output (I/O). All inputs that enter the Controller board pass through input multiplexing with two exceptions, V-BAT (keep-alive voltage to the CMOS RAM's), and INT (interrupt line from the A61 HP-IB board to the PIA). The rest of the inputs are passed into four 8:1 input data selector chips (U39-U42) for data lines DØ-D3, or into two dual 4:1 selector chips (U36 and U38) for data lines D4-D7. The processor will select one combination of eight inputs by setting a specific code on address lines AØ, A1 and A2 and then strobing the data selectors to put the selected inputs on their respective output lines DØ-D7 for transfer to the processor. An eight-position DIP-switch (S2) provides special test inputs to the processor as well as identification of instrument model (3586A, B, or C) and whether Option 003 (Impairments) is installed. A five-position DIP-switch (S1) provides a manual processor reset and additional test capabilities (see Service Group C). Comparators U37a-U37d are level-shifters for inputs which are not at TTL levels.

8-259. All outputs from the A60 board are controlled through Ports A and B of U18. The processor sets up an output operation by placing the output gating code on the data bus and the destination (Port A or B) on address lines AØ and A1. The PIA is then enabled by setting A11 HIGH and $\overline{CS2}$ LOW. R/$\overline{W}$ is now set LOW (write command) and the next $\phi 2$ pulse on line E clocks the gating code into U18 and directs it to the correct port. For example, if Port B were the destination, the gating code would be placed on PIA output lines PB0-PB7. The next negative-going pulse on line E is now passed to U18 pin 19 (CB2) and gated to one of two output decoders (U30 or U31) as determined by U18 pin 13 (PB3). If PB3 is HIGH, the pulse is gated through U30 and one of its output lines (YØ-Y7) as selected by the gating code on PBØ, PB1 and PB2. If PB3 is LOW, the pulse is gated through U31 in the same fashion.

8-260. When selected, pulses Y1 or Y7 from U31 are sent to latches U21 or U22 respectively where they gate data from U18 Port A (PAØ-PA7) to other circuits in the instrument. U31 outputs Y2 and Y6 are used to convert parallel data (PAØ-PA7) arriving at U19 into serial data for circuits requiring this form of data. A typical serial output to the A70 (Option 003) board would occur as follows. The processor would place a clock steering command on PAØ-PA7 and latch it into U21. U21 pin 6 would then enable the OPTION CLOCK gate U33c as soon as an output code from Y7 of U31 latched the Port A data into U21. The processor would then change PAØ-PA7 to the data destined for A70. Y6 of U31 now causes the data to be latched into the shift register and then eight successive pulses on the Y2 line clock the data over the serial output line of U19 (pin 9). In between each pulse of Y2, the processor must also generate the OPTCK signal by selecting output Y3 of U31. This signal shifts in the serial data stream, one bit at a time, into a serial-to-parallel shift register on the A70 board. The Y3 output is a general purpose clock that is steered by various enables being output by U21, and Y4/Y5 go to the FN Logic Chip on A30 as Instruction Valid (FIV) and External Clock (FDC) lines respectively. The YØ output is used both as a Display Clock on the A98 board and also as a reset to Display Refresh Timer U20. Lines YØ-Y6 of U30 go directly off of A60 as control lines or latches for other circuits.

8-261. While Port B of U18 usually provides the control function for output operations, Port A usually provides the actual data to be sent to other circuits. During normal operations, the processor will determine that some data must be output to a specific circuit. For example, a frequency change of several MHz would require a new $\div$N number for the Step loop. The processor would first direct a new $\div$N number over the data bus to the PIA for Port A (PAØ-PA7) and then direct an output gating code to Port B that would select the Y1 output of U31. The Y1 output of U31 would then latch PAØ-PA7 data into U22 for transmission to the A50 board.

8-262. Some parallel output data, like the serial data mentioned above, is latched in at the board it is directed to. For example, changes to various display annunciators on the front

panel are handled by sending PAØ-PA7 data directly from buffer U1 over to the A98 board and then selecting Y3, Y4, Y5 or Y6 of U30 to latch the data over on the A98 board into the correct annunciator group (ANNUN Ø-ANNUN 3).

8-263. Whenever data must be transmitted across the ground isolation barrier (refer to paragraph 8-111), some signal isolation is necessary. Photo-isolator A99U1 and Pulse transformers A99T3, A99T4 and A99T5 provide this isolation feature for selected signals.

8-264. Interrupts. When the HP-IB board (A61) has input data for the processor, A61 will set the INT line HIGH and U18 will then set $\overline{\text{IRQ}}$ B LOW to interrupt the processor for the HP-IB operations. The basic timing signals for all other processor operations come from U20 which generates a timing pulse at approximately 1900 Hz. This pulse, occurring on the INT CA1 line causes U18 to set the $\overline{\text{IRQ}}$ A line LOW, interrupting the processor. Each time the PIA sets the $\overline{\text{IRQ}}$ A or $\overline{\text{IRQ}}$ B line LOW, it places a status word on the data bus lines DØ-D7 to identify to the processor the source of the interrupt request. The processor sets R/$\overline{\text{W}}$ HIGH, samples the status word and, if HP-IB, requests a data word from the input multiplexers for HP-IB. If display timer is the source, the processor then checks various program counters for subroutine executions.

8-265. Displays/Keyboard - A98 (Service Group C).

8-266. Displays. The front panel displays are selected and updated in one of two ways, either one-shot or pulsed display refresh. The panel annunciators such as dBm, OVLD, SCALE, TALK, LISTEN, THSHLD, OFFSET, etc., are one-shot, i.e., they are selected on or off and not disturbed again unless they must be changed from their present condition. To reduce steady-state power consumption, however, the measurement and frequency digital LED display areas and the switch LED's (red lights in the center of some keys) are refreshed at a scan rate of about 100 Hz. Prior to each refresh clock pulse the numerical value segments for each digit are re-latched into the segment drivers and the next pulse then illuminates the correct number (Ø-9 plus decimal point) for the selected digit (DS1-DS14). Since every digit is pulsed once during a single display scan (or 100 times per second), it takes less than 10 milliseconds to update the entire display if a change occurs. The switch LED's (called Key Annunciators) are pulsed on in five groups of seven or eight at a time as part of the scan. The scan is fast enough that no flickering is discernible and the displays and switch LED's appear to be on at all times.

8-267. Digit display data enters the A98 board as follows. The processor on the A60 board puts the proper segment pattern of the first digit (DS1) on data lines PAØ-PA7 of A98J1 and the display clock line (DSP CLK) latches the data into A98U7. The processor now places a single bit (HIGH) on the display serial input line (DSP SI) and the next clock pulse on DSP CLK sets U1(3) HIGH and U4(1) LOW which selects DS1. The pattern latched into U7 determines the segments to be illuminated on DS1, the proper drivers (Q1-Q8) are turned on and the correct number is displayed on DS1. DSP CLK is about 1900 Hz.

8-268. The processor changes the segment pattern on PAØ-PA7 to that for DS2 and sets DSP SI to LOW prior to the next clock pulse. The next clock pulse on DSP CLK shifts the HIGH on U1(3) to U1(4) and also latches the new segment pattern into U7. This lets U4(1) go HIGH (turning OFF DS1) and U4(4) go LOW (turning on DS2). This process continues as DSP CLK shifts the single pulse down and out of U1 into U2, through U2 until the last digit (DS14) has been scanned, then through the switch LED groups in the last part of U2 and the three outputs of U3. The clock pulses are about .5 ms apart and the whole scan takes

19 pulses or about 10 milliseconds to complete, therefore the refresh rate is about 100 Hz. Only one display digit (DS1-DS14) or one group of switch LED's is actually on and drawing current at any instant of time. The display scan rate can be checked via TF11 (paragraph 8-78).

8-269. The one-shot displays are much simpler to update. The processor sets the correct on/off pattern for a group of front panel annunciators on lines PAØ-PA7 and then sets the correct latch line LOW (ANNUN Ø-3). The annunciators now remain in this state until a change to one of them occurs at which time only the respective group driven by U8, U9, U10 or U11 is updated.

8-270. Keyboard. Simultaneously with the display refresh of digits DS1-DS8, the bit being shifted down the output lines (QA-QH) of U1 is also applied to eight keyboard switch groups (A-H). There are eight switches in each group (except only seven in group B) for a total of 63 front panel switches. In their static condition (no keys depressed and scan refresh not in process), key lines KEY Ø - KEY 7 are all LOW due to pull up resistors R17 (2-9) holding + 5v on the inverting buffers of U14. When scan refresh begins and switch group A inverting buffer U12(12) goes LOW, the processor samples key lines KEY Ø - KEY 7. If one of the switches in group A is pressed during the .5 ms clock pulse, the LOW at U12(12) will be seen through the switch and at the output of inverting buffer U14 as a HIGH on that respective key line.

8-271. For example, if switch group E were being scanned during the refresh cycle and the numeral "8" key was pressed, U14(5) would go HIGH (key line KEY 2). The processor knows it is scanning group E and since only the KEY 2 line is HIGH, switch SW 26 must be depressed (numeral 8) since it is the only switch in this 8 x 8 matrix common to both group E and key line KEY 2. The scanning process is fast enough that the processor actually looks at all the switches several times before the operator can remove his finger from the key. Switch "debounce" is handled by processor software so that each switch depression appears as only a single input from that key.

8-272. Rotary Pulse Generator (RPG). The RPG utilizes key lines KEY 6 and KEY 7 to provide an input to the processor. When the scan refresh pulse has been shifted completely through U1, U2 and is in the last position (QC) of U3, it also causes U15(5) to go HIGH which disables all of the U14 buffers. The processor again samples the key lines, but looks only at KEY 6 and KEY 7. If the RPG was turned either CW or CCW, one or both of the U16 flip-flops will be set and either U15 pin 13 (KEY 7) or both U15 pin 13 (KEY 7) and U15 pin 11 (KEY 6) will be HIGH. The processor will then increment or decrement the displayed frequency one step accordingly. When the refresh cycle starts over again and DSP SI goes momentarily HIGH, a pulse is applied to the CLR inputs of U16 to reset the flip-flops in case the RPG was used during the last refresh cycle and to make it available again for the coming cycle.

8-273. The A98 board has nine through-the-board traces for external circuits due to some front-panel-mounted components. The meter, speaker, volume control, headphone jack and power switch are physically mounted on the front panel or on the A98 board, but their respective circuits are discussed under the board titles where they are located.

8-274. Impairments - A70 (Service Group G).

8-275. The A70 board (Option 003), has three separate, functional circuits used for communications channel impairment measurements. Demodulated sideband audio from the A21 board comes onto the A70 board and is immediately paralleled into two of those cir-

cuits, Phase Jitter and Weighted Filter/Notch Filter. At the output of the Notch Filter circuit, the audio is then passed to an Impulse Measurement circuit. Additional functions of the A70 board include a TRUE RMS Detector/Logger circuit for level measurements of the processed audio, a Crystal Calibration Oscillator for the Weighted Filter, and some digital control circuits for use by the other board functions.

8-276. Phase Jitter. A measurement for phase jitter is performed on a specific test tone of either 1004 Hz (3586B) or 1010 Hz (3586A) which is usually applied to one end of a channel under test and then measured at the other end for phase modulation or "jitter" induced on the tone by the channel. This is done by demodulating the phase jitter component (sidebands) from the test tone and measuring their peak-to-peak amplitude. A DC voltage, directly related to the number of degrees peak-to-peak of the phase jitter present, is then passed to the A/D Converter (A22).

8-277. The incoming SSB DEMOD audio is bandwidth-limited for normal channel sideband audio, but is a 1004 Hz (BELL) or 1010 Hz (CCITT) tone for phase jitter tests. The tone is applied to a band-pass filter that is centered on 1000 Hz and is 1000 Hz wide so that it passes 500-1500 Hz. Over-all filter gain is +15 dB provided by the input amplifier U23a. The sinewave output of the filter is applied to a Limiter (U26c) which converts it to a squarewave from 0V base to +12V peak. (See Section VII (Δ 11).)

8-278. The 1004/1010Hz squarewave (with phase jitter) becomes one input to the phase detector half of U31. The VCO output is also 1004/1010Hz but without any phase jitter. The phase-locked loop (PLL) has a ÷ N = 1 and is therefore locked to the test tone frequency and tracks it even if it drifts. The exact frequency of the tone is not critical to phase jitter measurements because the next operation is to demodulate the phase jitter sidebands from their "carrier", the test tone, and to measure only the jitter. The frequency ranges of interest for phase jitter sidebands are from 4Hz to 300Hz and from 20Hz to 300Hz. The 4Hz and 20Hz lower limits of the jitter ranges are adjusted in the loop filter. The high end of the ranges are obtained by passing the output of U31(2) through a 300Hz Low Pass Filter (LPF). U25 is used to switch between the 4Hz to 300Hz measurement band and 20Hz to 300Hz measurement band. A HIGH on U25(2) selects the 4Hz to 300Hz measurement band. The VCO in U31 is enabled only when Q4 is turned on under control of the processor (ϕ JITTER selected on the front panel). See Section VII (Δ 11).)

8-279. The last stage of the LPF is an adjustable gain amplifier. It is used to obtain the proper scale factor (6°/1.0 volt) for the phase jitter DC output to a voltage-divider circuit on the A/D Converter (A22). The only signal remaining at the output of the LPF is the phase jitter sidebands. This signal has two paths, one of which is through a buffer (U30b) to a rear panel BNC connector. By observing this signal on a spectrum analyzer, a scope, or a frequency counter, analysis can be made of the frequency source of the phase jitter present in the channel. The second path is through a peak-to-peak detector which converts the AC signal to a DC signal whose amplitude represents the number of degrees of phase jitter present on the test tone. U42 and U43 provide a means of speeding the discharge time of holding capacitors C150 and C151 before a new measurement is made.

8-280. An additional output of U31 (pin 10) is a DC voltage related to the VCO error voltage. This voltage is fed to a dual-comparator circuit used as a Valid Frequency Detector. U26(1) is normally HIGH and U26(13) is normally LOW, therefore U26(2) is normally HIGH (frequency valid). If the VCO is running outside a 100 Hz "window" of 960-1060 Hz, either U26(1) will trip LOW (frequency > 1060Hz) or U26(13) will trip HIGH (frequency

< 960Hz) and U26(2) will trip LOW (frequency invalid). This signal (L) JITTER INVALID is passed to the processor which displays the error code E 2.3 in the MEASUREMENT/ ENTRY display area as long as the tone is invalid and the ϕ JITTER measurement mode is selected. An adjustment is provided (R181) to move the center frequency of the 100Hz window. (See Section VII (Δ 11)).

8-281. Weighted Filter/Notch Filter. The SSB DEMOD audio is also applied to the input of a weighted filter with a +6 dB gain overall. Whenever the WTD 3100 Hz bandwidth is selected, either a C-Message filter (3586B) for Bell systems or a Psophometric filter (3586A) for CCITT systems is switched in by U37. When no weighting is desired, an alternate path through a +6 dB amplifier (U1a) is provided. The audio is then applied to a buffer (U4a) where again two paths are possible. When the NOISE/TONE measurement mode is selected, a notch filter, which uses gyrators to simulate the large inductance values required to obtain low-frequency, narrow notch (high Q), is switched in to notch out the tone. The notch filter has unity gain and is centered on 1010 Hz. The bandwidth is 30 Hz at the −60 dB points so it eliminates the 1004 Hz tone used by Bell systems also. In all other measurement modes (except IMPULSE), the audio bypasses the notch filter. Switching is performed by U38.

8-282. The audio is now applied to a +7.7 dB gain buffer (U8a) from which parallel paths take it to the True RMS Detector/Logger, to the Impulse circuits, and also to the speaker amplifier.

8-283. The Logger Range Expander circuit conditions and shifts the dynamic range of the audio so that it is within the input limitations of the Detector/Logger chip (U22). The output of U22 is a logarithmic DC voltage representing the true RMS amplitude of the audio signal present at the output of U8a. This signal is amplified by U10a and the voltage is clamped by U10b to prevent it from ever exceeding about +40 millivolts, since the A/D operates only on negative input voltages. Q3 provides a larger time constant selection for U22's RMS detector when AVErage is selected on the front panel.

8-284. The second output of U8a is applied through R52 to the A21 board which routes it to the Volume control, the speaker amplifier and on to the speaker. The third path is to the Impulse circuits.

8-285. Impulse Noise Circuits. Impulse noise measurements are made for communications channels that carry data. For impulse measurements, the SSB DEMOD audio may include the 1004/1010 Hz tone. It is passed through the weighted filter, if selected, but it is always passed through the notch filter. The resulting channel noise is then compared to a threshold voltage that is selected by the operator (in dBm) from the front panel, digitized by the processor and then changed to an analog voltage by a D/A Converter and input to a voltage comparator as a fixed reference level. Any impulse noise spikes in the channel noise that exceed the reference level (threshold) are counted and passed to the processor. When a predetermined time period set by the operator has passed, the processor freezes the total count and displays it to the operator. A dead-timer circuit controls the maximum number of impulse spikes that can be counted per second (7 in the 3586B, 8 in the 3586A).

8-286. The impulse circuits have a total dynamic range of 60 dB. Of this, 45 dB (in 15 dB steps) is in the path of the channel signal and 15 dB (in .25 dB steps) is the D/A Converter range. The AC channel signal from the notch filter is applied first to a Ø dB or +15 dB amplifier (gain determined by U35b) and then to a Ø dB or +30 dB amplifier (gain determined by U36). The signal is then applied to a unity-gain, full-wave rectifier stage which

folds the negative half of the channel noise signal over on top of the positive half and then inputs it to the comparator. Thus, all positive and negative impulses in the channel will appear as positive spikes at the comparator.

8-287. The other input to the comparator originates as a digital input to D/A Converter U18 from the processor. This is the reference level, or threshold value, that the operator has selected to compare the channel noise to. U41 converts the D.C. current out of U18(4) to a D.C. voltage at U19(3). The static condition of U19(7) is normally LOW (channel noise below threshold setting). Any impulse noise spike of long enough duration and high enough amplitude to trip U19(7) HIGH will trigger the "one-shot" circuit in the Dead Timer. The Q output of U20 then holds the input to the one-shot LOW until the time constant set up by C83, R98, and R97 allows the one-shot to reset. This time delay is 143 ms (7 per second maximum) for the Bell system (3586B) and 125 ms (8 per second maximum) for the CCITT system (3586A). Meanwhile, the Q output of U20 has incremented the counter in U21, which is a 4 bit counter (maximum count = 2^4 = 16). The counter is sampled once every second by the processor to prevent overflow. U35a allows a faster time constant to be implemented for impulse calibration during the CAL cycle.

8-288. Calibration Oscillator. The USB and LSB oscillators used as the SSB LO during normal operations produce an 1850 Hz tone when beating against the second IF frequency. This tone would not be usable for calibration of the weighted filter since some of its level would be clipped by the filter. Therefore a separate calibration oscillator is used to generate an SSB LO frequency in CAL that will be 1000Hz (3586B) or 800Hz (3586A) after mixing with the second IF frequency and which will provide accurate calibration of the weighted filter. (See Section VII (Δ 11).)

8-289. U40(10) is normally held LOW inhibiting the CAL OSC from reaching the A22 board. When U40(10) goes HIGH, the CAL OSC signal is then passed through U40 and on to the A22 board. The frequency of the CAL OSC signal (1.6625MHz/3586B) (1.6425MHz/ 3586A) is divided by 10 on the A22 board to produce 16.625kHz or 16.425kHz which will become the SSB LO frequency. When beat against the second IF (15.625kHz), a 1000Hz or 800Hz audio tone is produced which becomes the SSB DEMOD signal input to the A70 board in CAL. (See Section VII (Δ 11).)

8-290. Digital Control. All of the control lines which set up the various analog switches on the A70 board, together with the digital threshold level selected for impulse measurements are input in a serial data stream from the processor. The serial data comes in to U15 and is shifted through U15, into U14 and through U14 by the option clock line OPTCK. Once the entire data stream is present, the LATCH line latches the data into U16 and U17. U16 now sets up all the analog switches on the board and U17 provides the impulse reference level for the D/A Converter.

8-291. Frequency Reference - A40 (Service Group H).

8-292. The Frequency Reference board provides most of the frequencies used throughout the instrument as references. A 50 MHz oscillator is used as the base frequency and all other frequencies are obtained by dividing 50 MHz by 5 or by 10 in successive stages until each desired frequency is obtained. Available frequencies are: 50 MHz, 10 MHz, 2 MHz, 1 MHz and 100 kHz.

8-293. The 50 MHz reference is obtained from a voltage-controlled crystal oscillator (VCXO) made up from Q90 and Q91 with Y90 (50 MHz) and varicap CR91 providing a positive feedback path. A D.C. control voltage from U55 is used to change the capacitance

of CR91 and thereby maintain the 50 MHz reference accurately. CR90 provides amplitude limiting for the oscillator output at about one diode voltage drop (peak).

8-294. The VCXO output feeds a Buffer/Level Shifter circuit which raises the sinewave to an ECL level signal. Other ECL level buffers (U90, U93) then drive three 50MHz outputs to the A15 and A11 boards and to a test jack. (See Section VII (Δ8)).

8-295. A fourth 50MHz path is to a ÷5 chip (U53) where three outputs of 10 MHz are obtained. One of these goes to a rear panel BNC labeled "10 MHz" for phase-locking other instruments to the 3586 frequency reference. One 10 MHz path from U53 (pin 4) is buffered by U52b and passed through a low-pass filter to obtain a clean sinewave. The signal is then squared up by buffers (U3a and U3b) to drive a +10 dB amplifier and obtain the desired amplitude level. The output of T1 has some harmonic distortion remaining which is reduced by another low-pass filter and then passed to the rear panel BNC connector.

8-296. A second 10 MHz path from U53 (pin 2) is buffered and then passed to the A50 board. C15 removes the DC component and shifts the signal down around a Ø volt reference.

8-297. The third 10 MHz output of U53 (pin 3) goes to a ÷10 chip (U31) where two outputs of 1 MHz and one test jack secondary output of 2 MHz are obtained. Both of the 1 MHz outputs, being out-of-phase, are used to drive an ECL/TTL level shifter (Q31 and Q30). The resulting TTL signal at 1 MHz is again divided by 10 in U30 to obtain 100 kHz, which is passed through a differentiator circuit to obtain a very narrow pulse (about 30 nanoseconds wide). This pulse is used in the Fractional-N Phase Detector as the reference input.

8-298. One of the 1 MHz outputs from U31 (pin 14) is also used to provide a 1 MHz reference to three other boards. It is first buffered by U32 and then shifted in level from ECL to CMOS by U33b. Three buffered outputs go to the A15, A22 and A11 boards. The output to A11 is also passed through a 20 dB attenuator circuit, a portion of which is located on the A11 board.

8-299. The 10 MHz at U53(4) is also fed through some buffers to a Phase Detector stage. The other input to the Phase Detector may come from an external source. Provision is made by 3586 Option 004 for a temperature stabilized (oven controlled) precision 10 MHz crystal oscillator (A16) with stability of 2 Hz/year. Any other stable external source may be used which is exactly 10 MHz or a sub-multiple thereof (e.g. 5 MHz, 3.333333 MHz, 2.5 MHz, 2 MHz, or 1 MHz).

8-300. The external source is connected through the rear panel BNC connector labeled "EXT REF INPUT 10 MHz ÷N" to a signal amplifier (U1) with input diode protection (CR1 and CR2). The signal level is shifted from Ø volt reference at the BNC input to a +3.5v (VBB) reference at the input to U1a. It is then amplified by U1b and out-of-phase signals at U1b pins 6 and 7 are passed to U2a. The pin 6 output is delayed slightly behind the pin 7 output so that U2a is turned on for only a short period. The pulses from the U2a out-of-phase outputs are applied to a differential amplifier (Q50 and Q51) in the Phase Detector stage, are amplified and then used to switch a bridge made up of diodes CR50-CR53.

8-301. If an external source is being used, the action of the phase detector bridge is to switch the 10 MHz signal from U53 into U54. C56 and R59 filter the signal so that only a DC level is seen as the input and output of U54. This analog signal is then buffered by U55 and used to control the frequency of the VCXO, locking it in phase to the external source. U54 has a voltage gain of 11 to pull up the low level of the 10 MHz signal from U53 to an amplitude that will control the VCXO.

8-302. If an external source is not used, the diode bridge is never turned on and U54(3) is essentially at ground potential. R78 is now used to set the VCXO frequency to exactly 50 MHz while manually shorting TP4 to TP5 to speed-up the normally very slow loop response time. Q55 is normally on, providing a very narrow bandwidth to the loop. If an external source is used that is outside this bandwidth, the output of U54 will swing positive and negative trying to lock on. The negative peaks will turn on CR55, charging C75 and turning off Q55. R88 (5.1 M ohm) now dominates the input impedance to ground instead of R83 (12.4 k ohms), widening the bandwidth momentarily so the loop can "speed-up" the lock onto the external source. When lock-on is achieved, the output of U54 will stop swinging, Q55 will again turn-on and the desired narrow bandwidth is achieved.

8-303. Whenever the loop is not locked but trying to lock-up (as described above) the charge on C75 will also bias off Q56. This will allow Q54 to turn on and the loop unlock indicator DS-1 will glow. At the same time, a LOW signal on the (L) REF UNLOCKED line to the processor will cause an error code (Err 8) to be displayed on the front panel.

8-304. 10 MHz Frequency Reference - A16 (Service Group H).

8-305. The Precision Frequency Reference 10 MHz oscillator (Option 004) uses the raw +23v from the A99 board as an input to its own +15v regulator to provide the proper voltage for U3. When the instrument has been off for any significant period, at turn-on the oven will be cold and will draw a larger amount of current than normal from the regulator (U1) to warm up. R7 determines the sensing current level. U2(1) will trip HIGH, turning on the COLD OVEN light (CR1) on the board and also turning on Q3. When Q3 is on, the (H) $\overline{\text{COLD}}$ line to the processor will be LOW indicating a cold oven and the processor will illuminate the front panel OVEN annunciator. When the oven warms up sufficiently to trip U2(1) LOW, the light will go out on the board and the front panel annunciator will be off. When the oven is cold, Q2 shorts out the 10 MHz output from the oscillator since it is drifting until the oven temperature is stable.

8-306. HP-IB Interface - A61 (Service Group I).

8-307. The A61 board accepts instructions/data from the Hewlett-Packard Interface Bus (HP-IB) and transmits this information to the processor on the A60 Controller board. It also accepts data from the A60 processor and puts this information on the HP-IB for transmittal to other instruments. The A61 board has its own microprocessor to facilitate the rapid handling of I/O data to and from the HP-IB and the A60 processor.

8-308. The timing for the A61 board is established by an internal clock circuit of the microprocessor (U1) utilizing an external coil (L3) to achieve a reference clock frequency of approximately 4-5 MHz. U1 internally divides this clock by 15 to obtain the ALE address strobe at U1(11) of approximately 300 kHz.

8-309. The A61 processor (U1) uses the same eight parallel lines (called BUS Ø-7) for transmitting both address and data words and for accepting both instructions and data. For example, during an "instruction fetch" the computer places address bits AØ-A7 of the next instruction to be executed on the BUS Ø-7 lines and address bits A8-A10 on Port Two (P2) lines Ø-2. On the next Address Latch Enable (ALE) clock pulse, U21 latches in the address to ROM U29. When the Program Store Enable line ($\overline{\text{PSEN}}$) goes LOW, the Chip Select line ($\overline{\text{CS}}$) on U29 enables the ROM output. U29 now places the instruction word found in the selected address on the Bus where it is read by U1 and then executed.

8-310. When the A61 processor has data for the A60 processor, it first places a status/control word on the Bus and latches it into U21 with the next ALE clock pulse. It then places the data word on the Bus and strobes the bus write line ($\overline{WR}$) with a narrow negative pulse. On the trailing edge of this pulse, U23 latches the data word into the A60 processor input lines and U22 latches the status/control word. The control word will set U22(9) HIGH which is the interrupt request line, (H) INTERRUPT, to the A60 processor. The A60 processor will then input the data word when it completes its present instruction cycle. The A61 processor is now in a "wait" state, waiting for the A60 processor to return one byte.

8-311. When the A60 processor has data to return to the A61 processor it places the data word on lines PAØ-PA7 and then sets the (H) LOAD BUS line HIGH to latch the data into U24 and to notify the A61 processor (via U25b) that a word is available for transfer. For U24 to place the data on the Bus, both inputs to U19b must be HIGH which will trigger the control enable line (CNTRL) on U24. U22(2) will already be HIGH as part of the "handshake" that occurred when A61 passed data to A60. U1 now gates U19b on (output LOW) by strobing the read ($\overline{RD}$) line with a narrow negative pulse. U24 now places the data on the Bus and the processor reads it into U1.

8-312. At turn-on, the processor reads its own HP-IB address code from the address switches on the A62 board which are physically located on the rear panel. To do this, U1 outputs a control word to U22 which places a LOW at U22(2). This removes the enable from U19b but provides the enable to U19a through U16b. Now when $\overline{RD}$ is pulsed, U26 passes the setting of the address switches over the Bus to U1. U1 then passes this address word to the A60 processor. If the front panel LOCAL key is pressed, the processor displays the 3586 address code in the FREQUENCY/ENTRY display area. Also, at turn-on only, if A62S1(1) is in TEST, the A61 processor performs an automated test procedure determined by the other switch positions on A62S1 (see Service Group I for a description of these tests).

8-313. When an instrument designated as a "controller" on the HP-IB makes a change to the HP-IB system configuration, it will set the attention (ATN) line true (LOW).

NOTE

All HP-IB control lines and data lines use LOW = TRUE logic as defined by standards document IEEE-488. LOW = 1 and HIGH = Ø.

When the ATN line goes true at the A61 input, this LOW is passed through U5 to the CLK 1 input to U30 which normally has both of its flip-flops in a "clear" state. $\overline{Q1}$ now flips LOW which trips the enable lines (pins 10 and 12) to U18c and U18d LOW and the (L) NRFD and (L) NDAC lines become TRUE, inhibiting data transfer until U1 is ready. The U30 $\overline{Q1}$ output is also applied through U9 as a LOW to the T1 input of U1 where it interrupts the processor. U1 now outputs a control word to U22 which places a LOW at U22(5). This LOW is passed through U31a to the CLK 2 input at U3(13). The CLK 2 input flips $\overline{Q2}$ LOW which trips CLR 1 and flops $\overline{Q1}$ back to HIGH enabling U18c and U18d again. Q1 flops LOW tripping CLR 2 and $\overline{Q2}$ flops HIGH. Both U30 flip-flops are now again in the clear state. At this time, all the I/O bus transceivers (U2, U3, U4 and U5) must be set up to the input (listen) state. This is accomplished by ATN true, producing a HIGH at U20(5). U20b is enabled with A62S1(2) in REMOTE, therefore U20(6) is HIGH and this HIGH is passed through U17a as an enable LOW at all the DIO1-DIO8 gates (U14 and U15). Bus pull-up resistors (R3) now cause all the U1 (Port One) data lines (PIO-PI7) to be HIGH. These lines being

HIGH make the outputs of U6, U10 and U11 HIGH. Therefore bus transceivers U2, U3 and U4 for HP-IB data lines DIO1-DIO8 are all HIGH at the point between the OR gates and the buffer amps. This HIGH acts as a bus pull-up at these points and, since the HP-IB uses LOW = TRUE logic, an incoming LOW on any of the HP-IB data lines is enabled as an input to the A61 board.

8-314. The "handshake" control lines for the listen state are set up individually by U1. NDAC is true via a LOW at U17(5), with U17(6) already LOW, causing a LOW at U18(9 and8). NRFD is false via a HIGH at U17(8) causing U18(13 and 11) to be HIGH also, U18(12) already being HIGH. DAV must be enabled by U1 in the listen state and this is accomplished by a HIGH at U10(5).

8-315. The (H) TALK, (H) LISTEN, (H) REMOTE and (H) SRQ lines to A60 notify the processor to light the corresponding status annunciator on the front panel. The (H) TALK and (H) LISTEN lines also control the direction of HP-IB data and handshake lines on the A61 board when the HP-IB controller commands the 3586 into either of these modes. In addition to notifying the A60 processor that the A61 processor has data for it, the (H) INTERRUPT line also resets U25b in preparation for the A60 to return data to A61.

8-316. When the 3586 is not in REMOTE and the HP-IB controller wants the 3586 in REMOTE, the controller sets the ATN line true, puts the 3586 "Listener" address on DIO1-DIO8 and sets the remote enable (REN) line true. Then it sets data valid (DAV) true. When DAV goes true, U1 samples the word from DIO1-DIO8 and checks U1(22) to see if REN is true. It also checks to see if the 3586 is being addressed by comparing the sample word to the present address switch settings on A62S1. If the sample address and the 3586 address are not the same, the HP-IB is ignored and the 3586 stays in LOCAL. If they are the same, U1 places the 3586 in LISTEN. If REN is true, U1 also places the 3586 in REMOTE.

8-317. If the 3586 is already in REMOTE, U22(6) will be High enabling U20a. If REN now goes false, U20a will trip U17(13) LOW which generates an interrupt to U1 on the $\overline{\text{INT}}$ line (pin 6). Also if the controller sets the interface clear (IFC) line true, it will also trip U17(13) LOW to generate an interrupt. The processor examines U1(21) and U1(22) to see which line (REN or IFC) caused the interrupt. If REN is false U1 takes the 3586 out of REMOTE. If IFC is true TALK or LISTEN are cleared out (if selected).

8-318. The 3586 can act as a partial controller if the A62S1(2) switch is put in the TRACK position. This will change the state of several gates and transceivers and allow the 3586 to control the ATN and REN lines. In this mode, the 3586 puts out continuous frequency information only, as a "Talker" on the bus. U1 samples the position of A62S1(2) periodically anytime the HP-IB is idle (not in REMOTE) to see if this switch has changed position.

8-319. For normal operation in REMOTE as a talker, U1 reconfigures the gates via a HIGH at U22(18) and U19(12) to pass data on to the HP-IB, rather than accept it from the HP-IB.

8-320. All normal data transfers on the HP-IB, whether in or out, take place with a "handshake" of control line states between the talker and the listener(s). This sequence occurs as follows:

1. All listeners set (L) NDAC true and (L) NRFD false.
2. Talker places data word on DIO1-DIO8.
3. Talker sets (L) DAV true.
4. All listeners set (L) NRFD true and sample DIO1-DIO8.

5. All listeners set (L) NDAC false.
6. Talker sets (L) DAV false and clears DIO1-DIO8.
7. All listeners set (L) NDAC true and (L) NRFD false and the cycle repeats with a new data word.

8-321. Power Supply - A80, A99 (Service Group J).

8-322. The A80 board is primarily a voltage regulator board for the three main supply voltages (+12vdc, −12vdc and +5 vdc). The source of the inputs to A80 for these voltages is the power supply circuitry on the A99 Motherboard and some chassis-mounted components.

8-323. Instrument AC power is selectable, with a choice of 110, 120, 220 or 240 VAC @ 48-66 Hz. Two switches, S1 and S2, physically mounted on the rear panel allow the operator to choose one of the four above voltages for a fused (F1) input to T1. S3 provides thermal cutout protection if the ambient temperature exceeds 105°C. A fan (B1) is on anytime the instrument power switch (A98S300) is in the ON position, energizing K1. Secondary windings of T1 drive three diode-bridge, full-wave rectifiers. CR1-CR4 on the motherboard (A99) provide +16.5v and −16.5v to the +12v and −12v regulators respectively. CR5-CR8 furnish +8v to the +5v regulator and CR9-CR12 provide fused (F1 and F2) +23v and −23v to the A80 board as supply voltages for all the regulator circuits. Spare fuses (F3 and F4) are provided which are physically located on the mother board. In addition, the +23v feeds a +15v regulator (A99U2) which provides front panel probe power and feeds another +15v regulator on the A16 board (when installed). It is also the current source for charging a Nickel-Cadmium battery (BT1) on the A80 board. Q1, Q2 and Q3 are Darlington transistors which provide power regulation for the three main supplies.

8-324. In the +12v regulator, A80CR8 is the reference zener for the circuit with zener A80CR9 providing overload protection for amplifiers U1a and U1b. Zener A80CR3 provides −5.11v power for U1. When the instrument power switch is in standby (STBY), pin A22 of XA80 is "open" and Q1 is biased on through R17 and R18. This brings U1(5) down to approximately Ø volts and U1(6) follows, cutting off the +12v supply completely. Since the +12v is used as the reference input for the −12v and +5v regulators, all three supplies are turned off. The voltage present at the junction of R17 and R18 is applied through pin A22 over to the A98 board to light the STBY annunciator light (A98DS40) on the front panel.

8-325. When the power switch is changed from STBY to ON, the junction of R17 and R18 is grounded to chassis through the power switch, turning out the STBY lite, turning Q1 off and allowing the inputs to U1b to come up to the reference voltage across CR8. The voltage at TP1 now drives to +12v as set by R15 and all three main supplies are now turned on.

8-326. U1b is the voltage regulator while U1a provides current-limiting for the +12v supply. If the +12v supply were to become shorted, U1(1) would go LOW, turning on the red LED (CR2) and biasing Darlington transistor Q1 off to limit the current into the regulator. During normal supply operation, green LED CR5 is turned on and CR6 provides reverse bias protection for U1 in case the plus and minus supplies were to accidentally short to each other.

8-327. The −12v regulator operates in the same way as the +12v regulator, except that the reference for the voltage regulator (U2b) is the +12v supply through R38.

8-328. The +5v regulator operates in the same way as the +12v regulator, except that the reference for the voltage regulator (U3b) is the +12v supply through R58. Zener CR20 (near Darlington transistor Q3) provides over-voltage protection at +6.2v for the +5v supply.

8-329. The +23v input to A80 is also used to charge BT1, a 100 milliampere capacity NI-CAD battery which furnishes +2.5v of standby power to the CMOS RAM's on the A60 board. When all input AC power is removed from the 3586, the RAM's draw approximately 100 microamperes of current from BT1. With AC power connected to the instrument, even in STBY, a charging current of approximately 7 milliamperes maintains BT1 at full charge to provide about 30 days of battery life at the design load current when power is removed.

8-330. A transformer on the motherboard (A99T1) provides isolated power to the input section from the standard power supply buses of +12v, −12v, +5v, +15v and chassis (mainframe) ground. The isolated power supply buses of +12VI, −12VI, +5VI, +15VI and isolated ground are all used in the input section of the 3586A/B/C (see paragraph 8-111).

8-331. Motherboard - A99 (Service Group J).

8-332. The A99 Motherboard provides a common point of contact for all of the plug-in printed circuit boards in the 3586 and eliminates unnecessary wiring and cabling between circuits. The motherboard also provides connection points for chassis-mounted components such as the power transformer T1. See paragraph 8-321 for a discussion of the power supply circuits which are a part of the motherboard.

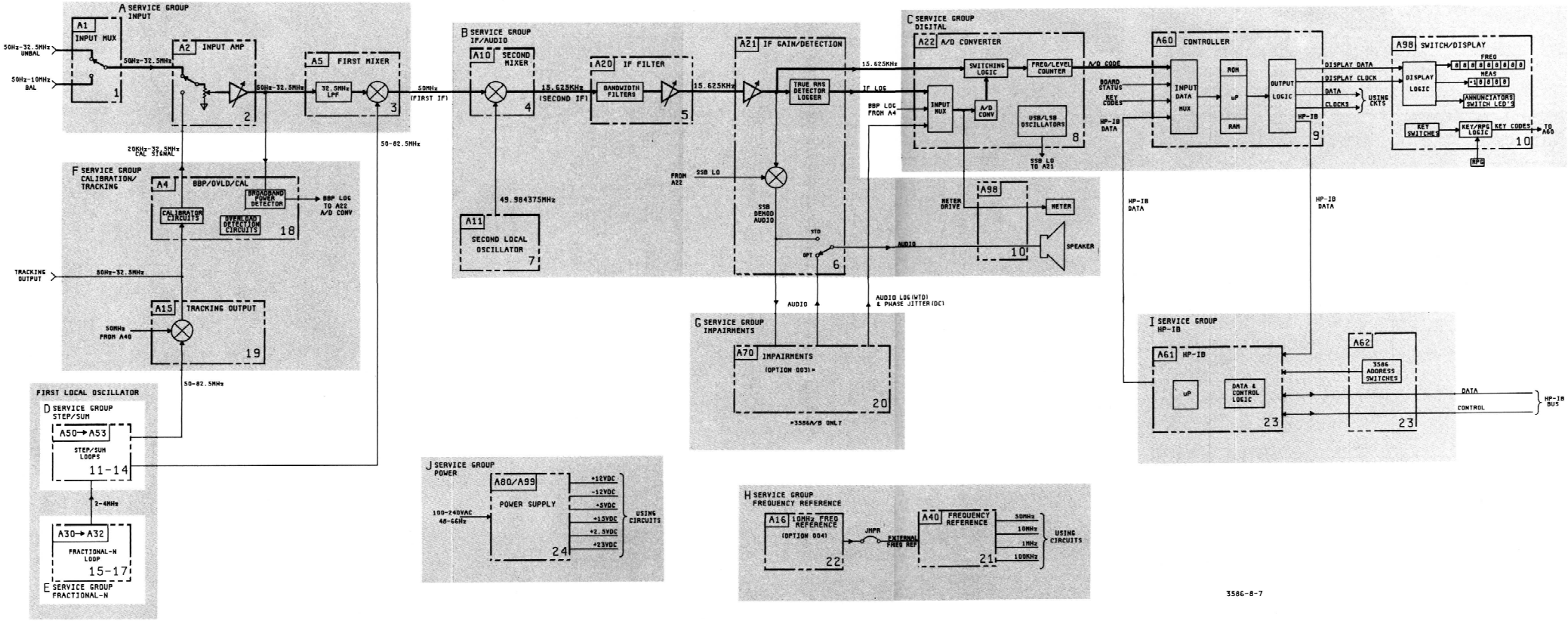


Figure 8-8. 3586A/B/C System Block Diagram

Table of Contents

8-333. GENERAL INFORMATION.

8-334. Service Groups; What They Are and How to Use Them.

8-335. The troubleshooting information provided in this section is divided into service groups. A service group is an arrangement of information pertaining to a particular assembly or group of assemblies which have a common functional operation within the instrument. The objective of the service group is to integrate all relative servicing information into a single location. Each service group contains schematic diagrams, functional block diagrams, troubleshooting data, and component locators for the circuit assemblies contained in the group. In addition, cross-references are provided within each group for applicable paragraphs on circuit theory and adjustment procedures for all assemblies in the group. Only the component parts list has been kept all together and separate in Section VI for ease in locating parts quickly.

NOTE

The functional block diagrams in each service group were designed as principal troubleshooting aids rather than merely to illustrate circuit operation.

8-336. The service technician can use the functional block diagram to isolate most problems to a single stage or small group of stages since all key test points, waveforms, voltages and digital codes are clearly shown. The technician may then use the schematic for voltage and resistance measurements to isolate the failed component(s). Component locator diagrams are included on the apron pages of both the functional block diagrams and the schematics to help locate test points and components quickly and easily. The functional block diagram is located behind the schematic so that it may be left unfolded and referred to as necessary while using the schematic. With this arrangement, both diagrams can be unfolded and easily worked with along with the troubleshooting data which overlays the apron pages.

8-337. As an added convenience, the appendix contains a copy of the 3586 System Functional Block Diagram along with duplicate copies of the Major Signal Chart and Turn-On Troubleshooting Flowchart. Once the faulty section of the instrument is identified and the functional block diagram for that section is unfolded, the system functional block diagram can remain unfolded for continued reference. This allows easy access to not only the schematic and functional block diagrams of a particular service group, but also to the system functional block diagram for an overview of any functional section with respect to the rest of the instrument.

8-338. Some technicians, experienced with the 3586, can generally recognize a particular problem symptom as being associated with a certain functional section of the instrument. Experienced service people can simply open the manual at the "Service Group Index" tab, quickly locate the correct service group and turn there for immediate troubleshooting.

8-339. Service Groups; How to Identify Them

8-340. Each service group is designated with a letter. The page numbers, figure and table numbers in each group contain the service group letter. Table 8-11 is a list of service groups which also provides cross-reference information for assemblies within each group.

Table 8-11. Service Group Cross Reference

Service Group	Assembly	Schematic Number	Assembly Designator	-hp- Part Number
A	Input Multiplexer (3586A)	1A	A1	03586-66506
A	Input Multiplexer (3586B)	1B	A1	03586-66501
A	Input Multiplexer (3586C)	1C	A1	03586-66507
A	Input Amplifier (3586A/B)	2	A2	03586-66502
A	Input Amplifier (3586C)	2	A2	03586-66503
A	Input Mixer (3586A/B)	3	A5	03586-66505
A	Input Mixer (3586C)	3	A5	03586-66509
B	Second Mixer	4	A10	03586-66510
B	IF Filter (2000Hz)	5A	A20	03586-66520
B	IF Filter (3100Hz)	5B	A20	03586-66523
B	IF Filter (1740Hz)	5C	A20	03586-66524
B	IF Gain/Detection	6	A21	03586-66521
B	Second Local Oscillator	7	A11	03586-66511
C	Analog/Digital Converter (3100Hz)	8	A22	03586-66522
C	Analog/Digital Converter (2000Hz)	8	A22	03586-66525
C	Analog/Digital Converter (1740Hz)	8	A22	03586-66526
C	Controller	9A/B	A60	03586-66560
C	Switch/Display (3586C)	10A/B	A98	03586-66594
C	Switch/Display (3586A Opt. 003)	10A/B	A98	03586-66595
C	Switch/Display (3586A STD)	10A/B	A98	03586-66596
C	Switch/Display (3586B STD)	10A/B	A98	03586-66597
C	Switch/Display (3586B Opt. 003)	10A/B	A98	03586-66598
D	Step Loop	11	A50	03586-66550
D	Sum Loop VCO	12	A51	03586-66551
D	Sum Loop Mixer	13	A52	03586-66552
D	Sum Loop Phase Detector	14	A53	03586-66553
E	Fractional - N ÷ N	15	A30	03586-66530
E	Fractional - N VCO	16	A31	03586-66531
E	Fractional - N Phase Detector	17	A32	03586-66532
F	BBP/OVLD/CAL (3586A/B)	18	A4	03586-66504
F	BBP/OVLD/CAL (3586C)	18	A4	03586-66508
F	Tracking Output	19	A15	03586-66515
G	Impairments (Opt. 003 - 3586B)	20A/B/C	A70	03586-66570
G	Impairments (Opt. 003 - 3586A)	20A/B/C	A70	03586-66571
H	Frequency Reference	21	A40	03586-66540
H	10MHz Frequency Reference (Opt. 004)	22	A16	03586-66516
I	HP-IB	23	A61	03586-66561
J	Power Supply (Regulator)	24	A80	03586-66580
J	Motherboard	24	A99	03586-66599

8-341. SERVICE AIDS.

8-342. The following paragraphs, figures and tables summarize all of the reference information that is common to all of the service groups. The service technician should familiarize oneself with all of this information to help decrease time wasted in troubleshooting, looking for information that is grouped together for his convenience.

8-343. Parts Location Aids.

8-344. The location of individual components on a printed circuit board is provided in each service group. Electronic parts not located on a specific PC board are listed under "Chassis Mounted Components" at the rear of Table 6-3 in Section VI. These include components physically mounted on the front panel such as the speaker, volume control and RPG. Also

included are rear panel items such as the fan, line fuse, etc. and some chassis-mounted power supply components. At the rear of Table 6-3 are additional pages titled "Mechanical Parts", "Cable Parts List" and "Miscellaneous Parts" (knobs, key caps, etc.). Figure 6-1 is a mechanical parts exploded-view illustration and Figure 8-9 shows rear panel component locations. Figure 8-11 shows the P.C. board locations.

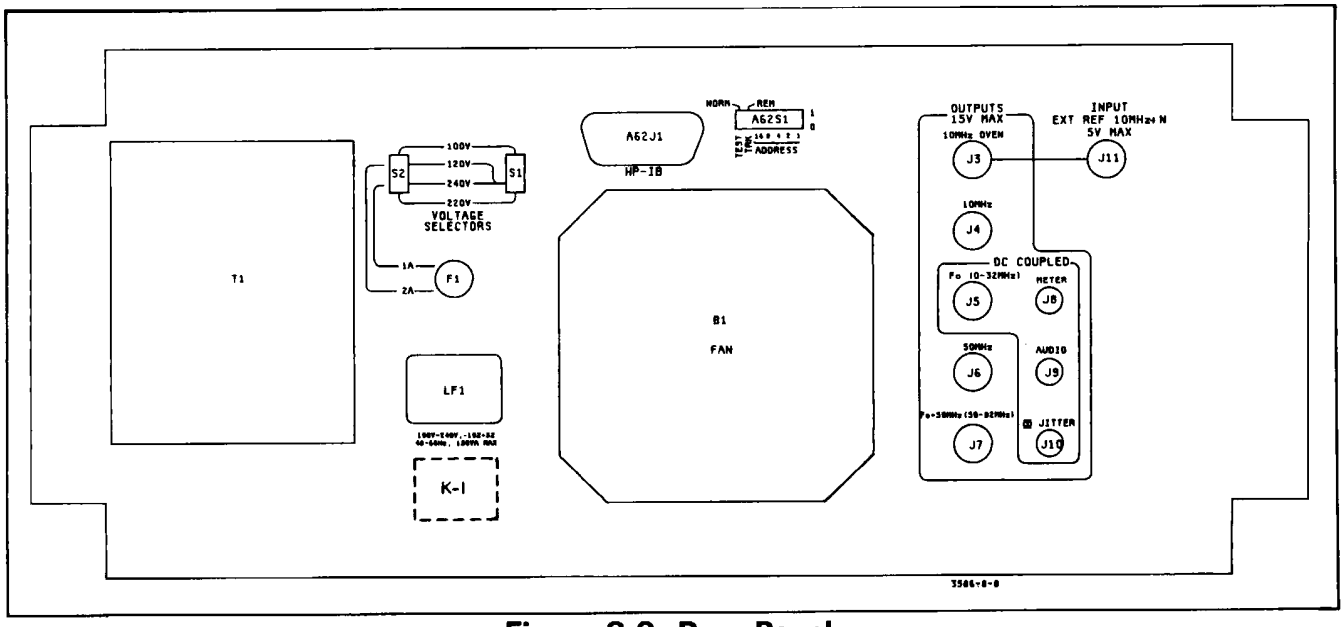


Figure 8-9. Rear Panel.

8-345. Both the origin and the destination for all cable assemblies are shown on the schematics and listed for each cable in the "Cable Parts List" of Table 6-3. In addition, all coaxial cables interconnecting PC boards have the local and the remote connectors identified at both ends on the PC boards. Table 8-12 also provides this data plus additional information.

Table 8-12. Cable Assembly Identification.

Reference Designator	-hp- Part Number	Color	Pins	Origin	Destination	Location
W1	03586-61612	--	14	A99J1	A98J2	Front Panel
W2	03586-61615	--	5	RPG	A98J3	Front Panel
W3	03586-61671	Black	1	A15J2	J5* "F_o(0-32MHz)"	Rear Panel
W4	03586-61674	Violet	1	A40J3	J4* "10MHz"	Rear Panel
W5	03586-61675	Red	1	A40J1	J11* "INPUT EXT REF"	Rear Panel
W6	03586-61676	White	1	A16J1	J3* "10MHz OVEN"	Rear Panel
W7	03586-61677	Blue	1	A40J5	A11J1	Top-Rear
W8	03586-61678	Gray	1	A40J4	A50J3	Top-Rear
W9	03586-61678	Gray	1	A51J3	A15J1	Top-Middle
W10	03586-61678	Gray	1	A51J1	A52J2	Top-Middle
W11	03586-61678	Gray	1	A50J1	A52J1	Top-Middle
W12	03586-61678	Gray	1	A2J3	A5J1	Top-Middle
W13	03586-61691	G/R#	1	A4J1	A2J2	Top-Middle
W14	03586-61691	G/R#	1	A1J1	A2J1	Top-Front
W15	8120-1538	--	3	Power	Line Filter (LF 1)	Rear Panel
W16	8120-2887	Blue	34	A61J1	A62J1	Rear Panel
W17	8120-2888	Blue	34	A60J3	A98J1	Front Panel
(Jumper)	1250-1499	Black	1	J3*	J11*	Rear Panel

* Rear Panel BNC Connectors (See Figure 8-9).
\# Gray/Red.

8-346. Controller Mnemonics.

8-347. Most inputs and outputs (both control and data) to and from the A60 Controller assembly are labeled by a mnemonic. To aid in identifying, locating the source, and describing the function of each controller I/O line, a complete mnemonic dictionary is provided in the appendix.

8-348. Adjustments Affected by Repairs.

8-349. Repairs to certain assemblies affect the calibration of the instrument and certain adjustments must be performed. Each applicable service group has a "Post-Repair Adjustments" paragraph that discusses required adjustments which may not be readily obvious to the service technician.

8-350. SERVICE HINTS.

8-351. Special Cables. It is not necessary to obtain or fabricate special cables to use the miniature gold connectors on top of the printed circuit assemblies. The BNC connector on the rear panel labeled EXT REF INPUT has a long enough cable attached to it to reach any of the small (50 ohm) connectors in the instrument. Simply disconnect it from A40J1 and then connect it to the desired connector. You may then use standard 50 ohm coax with BNC connectors to connect the 3586 to any other instrument using the EXT REF INPUT jack as an output or an input. In the same manner, the tracking output BNC labeled F_0 (0-32MHz) has a cable that will reach the five large gold connectors in the instrument (A15J2, A1J1, A2J1, A2J2, and A4J1). Use 75 ohm coax with the tracking output jack.

8-352. Tracking Output. The tracking output BNC on the rear panel labeled F_0 (0-32MHz) provides a handy signal source for test purposes. The output frequency should be the same as the front panel tuned frequency from 0-32.5MHz at 0 ± 1.0dBm (75 ohm impedance). You can connect a 75 ohm cable from the tracking output BNC to the 75 ohm input termination and you should read 0 ± 1.0dBm for any tuned frequency from 0-32.5MHz. Expect about 0.7dB loss at the higher frequencies if 50 ohm cable is used.

8-353. HP-IB Tracking. The 3586 has an HP-IB tracking generator mode in which it can command a signal source such as a 3336 or a 3335 to track any frequency set into the 3586. The 3586 is manually forced into a "TALK only" mode through rear panel switch selections and the above-mentioned sources can be forced into the "LISTEN only" mode to use this tracking capability. Refer to paragraph 8-I-5 for how to implement this mode.

8-354. Phase Locking. It is often possible to prevent lost troubleshooting time by always ensuring that critical test instruments such as counters, spectrum analyzers and signal sources are phase-locked to the 3586. This guarantees accuracy in all frequency-related measurements and can only help the service technician by eliminating confusion when an instrument is off-frequency by only a few hertz. This is especially important when using the 20Hz bandwidth filter in the 3586A.

8-355. Internal Source One. A precision internal calibration source is used to calibrate the instrument whenever the CAL cycle is active, but this source is normally switched in for only a few seconds. An internal test function (TF2 - paragraph 8-58) is available from the front panel to turn on this source and leave it on for test purposes. This function acts as a precision -40dBm or -20dBm source which is injected directly into the A2 Input Amplifier board thus bypassing the A1 Input Multiplexer circuits, a valuable tool for troubleshooting. The frequency of this source is the same as the tuned frequency of the 3586. See paragraph 8-59 for more information on the use of this function.

8-356. Internal Source Two. Another valuable troubleshooting/test tool is TF12 (paragraph 8-79). This function generates a constant 1MHz at −40dBm or −20dBm which is also injected into the A2 Input Amplifier. Since this source frequency is always 1MHz regardless of the tuned frequency of the instrument, by changing the tuned frequency (and thus the first L.O. frequency), the resulting second I.F. frequency can be varied as necessary to check bandwidth filter shapes (e.g., 3dB or "half power" points). See paragraph 8-80 for more information on the use of this function.

8-357. Problem Symptoms. Determining just what is wrong with the instrument is very important in determining troubleshooting strategy. The information contained under the heading "Turn-On Initialization and Milking the Front Panel" can help determine all of the problem symptoms that are discernable without ever removing the covers.

8-358. Schematic Reference Designations.

8-359. Figure 8-10 shows all of the standard reference designations used on schematics of functional block diagrams in the service groups.

8-360. General Schematic Notes.

8-361. Table 8-13 provides definitions for certain schematic symbology as well as some general notes applicable to all schematics.

8-362. Recommended Test Equipment.

8-363. Table 8-14 provides a list of Recommended Test Equipment.

8-364. Test/Function Capabilities.

8-365. Table 8-12A is a duplicate copy of Table 8-6 which has been placed here for ease in referral.

Table 8-12A. Test/Function Capabilities.

Paragraph	T/F Desig	Key Seq*	Test/Function	Exit**
8-55	TF 1	CF, Ø	Clears CAL constants	---
8-58	TF 2	CF, 1	Tracking CAL signal ON Input signal OFF	TF 3
8-66	TF 3	RO, 1	Input signal ON Tracking CAL signal OFF	---
8-67	TF 4	CF, 2	Hundredths digit ON	TF 5
8-68	TF 5	RO, 2	Hundredths digit OFF	---
8-69	TF 6†	CF, 3	First L.O. 1000 point sweep	MC
8-70	TF 7	CF, 4	RF Gain, 12 step cycle	MC
8-73	TF 8	RO, 4	−12 volt supply and A/D check (−125.50 to −130.30)(X.0938)	PWR
8-74	TF 9	CF, 5	IF GAIN, 22 step cycle	MC
8-77	TF 10	RO, 5	Right # = A/D converter offset Left # = Offset/Input difference	MC
8-78	TF 11	RO, 6	Display Scan Rate (100 ± 10 Hz)	MC
8-79	TF 12	CF, 7	1 MHz CAL signal ON Input signal OFF	AC
8-81	TF 13	CF, 8	Receiver Test 1.0-1.11 RF Gain 2.0-2.13 IF Gain 3.1-3.2 Detector/Counter 4.1-4.32 Flatness 5.0 Audio	MC
8-82	TF 14	CF, 9	Digital Test 10 dB ROM A (U12) 100 dB ROM B (U11) AUTO ROM C (U10) ENTRY ROM D (U9) AVE ROM E (U8) dBm ROM F (U7) (other) RAM	MC

* All key sequences include RECALL, • (decimal point) first.

CF = CNTR→FREQ RO = RDNG→OFFSET

** MC = MEAS CONT PWR = Cycle POWER switch AC = AUTO CAL

† Available in Revision "A" ROM software only.

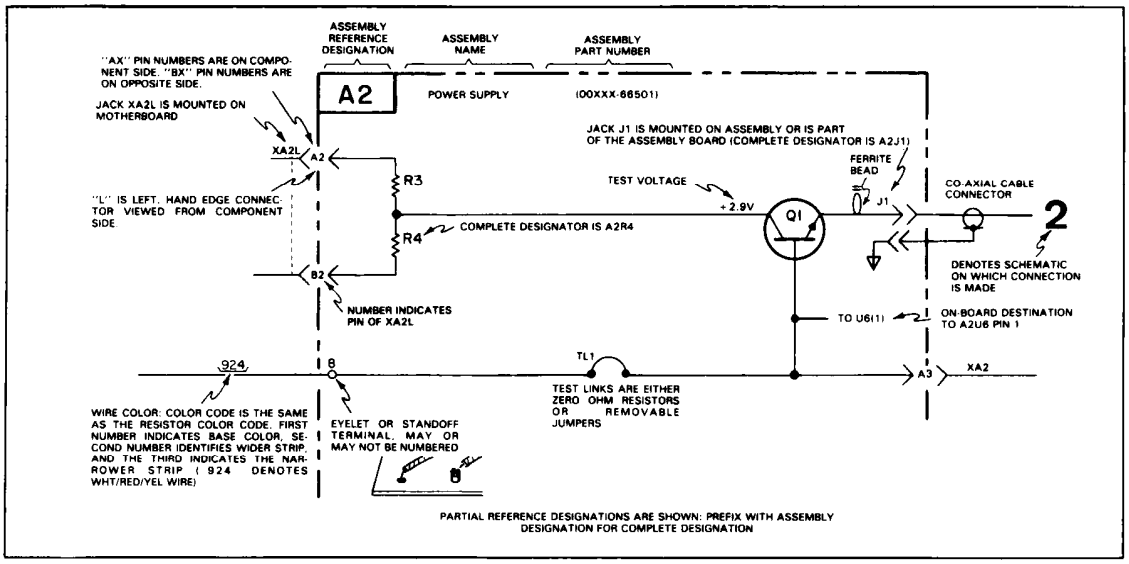


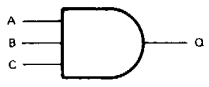
Figure 8-10. Reference Designations.

Table 8-13. General Schematic Notes.

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. PREFIX WITH ASSEMBLY DESIGNATION FOR COMPLETE DESIGNATION.
2. COMPONENT VALUES ARE SHOWN AS FOLLOWS UNLESS OTHERWISE NOTED.
   RESISTANCE IN OHMS
   CAPACITANCE IN MICROFARADS
   INDUCTANCE IN MILLIHENRYS
3. DENOTES EARTH GROUND. USED FOR TERMINALS WITH NO LESS THAN A NO. 18 GAUGE WIRE CONNECTED BETWEEN TERMINAL AND EARTH GROUND TERMINAL OR AC POWER RECEPTACLE.
4. DENOTES FRAME GROUND. USED FOR TERMINALS WHICH ARE PERMANENTLY CONNECTED WITHIN APPROXIMATELY 0.1 OHM OF EARTH GROUND.
5. DENOTES GROUND ON PRINTED CIRCUIT ASSEMBLY. (ELECTRICALLY CONNECTED TO FRAME GROUND).
6. I/S DENOTES ISOLATED (I) OR SIGNAL(S) CIRCUIT GROUND.
7. SCREWDRIVER GROUND.
8. DENOTES ASSEMBLY.
9. DENOTES FEEDBACK PATH.
10. DENOTES FRONT PANEL MARKING.
11. DENOTES REAR PANEL MARKING.
12. DENOTES SCREWDRIVER ADJUST.
13. * AVERAGE VALUE SHOWN, OPTIMUM VALUE SELECTED AT FACTORY. THE VALUE OF THESE COMPONENTS MAY VARY FROM ONE INSTRUMENT TO ANOTHER.
14. •NNI COMPONENT NOT NORMALLY INSTALLED ON PRODUCTION ASSEMBLIES.
15. \924/ DENOTES WIRE COLOR: COLOR CODE SAME AS RESISTOR COLOR CODE. FIRST NUMBER IDENTIFIES BASE COLOR, SECOND NUMBER IDENTIFIES WIDER STRIP, THIRD NUMBER IDENTIFIES NARROWER STRIP. (e.g. \924/ = WHITE, RED, YELLOW.)
16. ALL RELAYS ARE SHOWN DEENERGIZED. ALL ANALOG SWITCH IC'S ARE SHOWN NOT ACTIVE.
17. WAVEFORMS AND AC VOLTAGE MEASUREMENTS WERE MADE WITH RESPECT TO CHASSIS GROUND USING AN OSCILLOSCOPE WITH A 10:1 PROBE. THE VOLTAGE LEVELS SHOWN FOR THE WAVEFORMS ARE ACTUAL VOLTAGE LEVELS AND ARE NOT TO BE CONFUSED WITH OSCILLOSCOPE SETTING. THE VOLTAGE LEVELS SHOWN ARE NOMINAL AND MAY VARY FROM ONE INSTRUMENT TO ANOTHER. A VARIATION OF ± 10% IN MEASUREMENTS SHOULD BE ALLOWED. ALL WAVEFORMS SHOWN WERE AC-COUPLED UNLESS OTHERWISE NOTED. DC VOLTAGE LEVELS OF WAVEFORM TEST POINTS ARE INDICATED SEPARATELY.
18. DC VOLTAGE LEVELS WERE MEASURED WITH RESPECT TO CIRCUIT GROUND USING A DVM. THE VOLTAGE LEVELS SHOWN ARE NOMINAL AND MAY VARY FROM ONE INSTRUMENT TO ANOTHER DUE TO CHANGE IN TRANSISTOR CHARACTERISTICS. A VARIATION OF ±10% SHOULD BE ALLOWED.

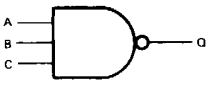
DENOTES BUFFER

DENOTES INVERTER



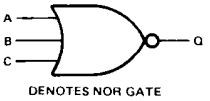
DENOTES AND GATE

A	B	C	Q
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	1



DENOTES NAND GATE

A	B	C	Q
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0



DENOTES NOR GATE

A	B	C	Q
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	0

DENOTES EXCLUSIVE OR GATE

A	B	Q
0	0	0
0	1	1
1	0	1
1	1	0

Table 8-14. Recommended Test Equipment.

Equipment	Critical Specifications	Application*	Recommended -hp- Model No.
Synthesizer/Level Generator	200Hz→65MHz, +10dBm→−80dBm, 00.01dB level resolution, frequency stability of less than 1 x 10^{-7}/year, calibrated attenuator.	P,A,R	3335A opt. 001 (special) K06
Synthesizer/Level Generator	40Hz→21MHz, +10dBm→−45dBm, frequency stability of less than 5 x 10^{6}/year.	P,A,R	3325A
Oscilloscope	100MHz BW	P,A,R	180A/1808A/1821A
Spectrum Analyzer	1kHz→32.5MHz, 60dB dynamic range.	P	141T/8553B/8552B
	1dB/Div Vertical Scale	A,R	3585A
Digital Multimeter	±0.1mV AC accuracy at 0.45V VRMS and 1kHz, ±10μV DC accuracy at 6mV, ±0.05Ω accuracy at 20Ω.	P,A,R	3455A opt. 001
RF Voltmeter		A,R	411A
RF Amplifier	+27dBm output, 15dB gain .5MHz to 32.5MHz.	P,A	Q-Bit, QB-188-LH-BNC with case and supply. Available from: Q-Bit P.O. Box 2208 Melbourne, Florida 32901
Frequency Counter	100MHz, 0.1Hz resolution.	A,R	5382A
Signature Analyzer		R	5004A
100kHz Low Pass Filter	≥48dB/Octave Roll-off, 75Ω input and output.	P	Available from: Allen Avionics 224E. 2nd St. Mineola, NY 11501
10MHz Low Pass Filter	≥48dB/Octave Roll-off, 75Ω input and output.	P	
Attenuator (Calibrated)	±0.03db with Cal. Sheet	P	355D
50ΩDirectional Bridge	≥30dB Return Loss ≥40dB Directivity	P	8721A
75Ω Directional Bridge	≥30db Return Loss ≥40dB Directivity	P	8721A opt. 008
124Ω Return Loss Coupler (3586B Standard)		P	Part No. 5061-1136
124Ω Return Loss Coupler (3586B opt. 001)		P	Part No. 5061-1137
150Ω Return Loss Coupler		P	Part No. 5061-1135
75Ω .5V Thermal Converter	Must include Calibration sheet	P	11051A, opt. 003
50Ω 1V Thermal Converter	Must include Calibration sheet	P	11050A, opt. 002
Frequency Doubler		P	10515A
(2) 50Ω/75Ω Minimum Loss Pads	50Hz to 32.5MHz, 30dB return loss.	P	11852A (pad) 1250-1473 adapter 1250-1536 adapter

* P-Performance Tests; A-Adjustments; R-Repair.

Table 8-14. Recommended Test Equipment (Cont'd).

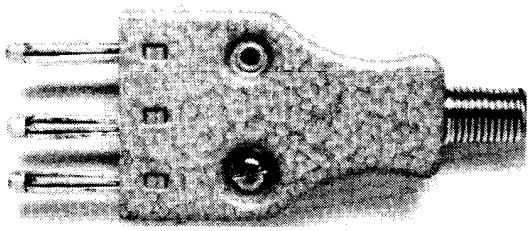
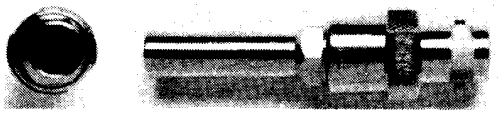
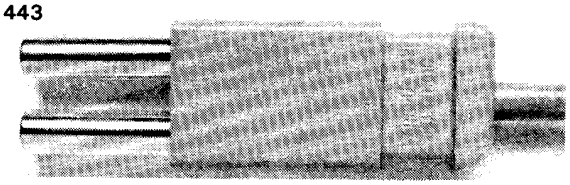
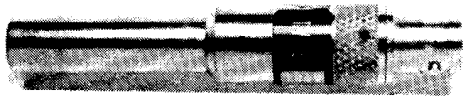
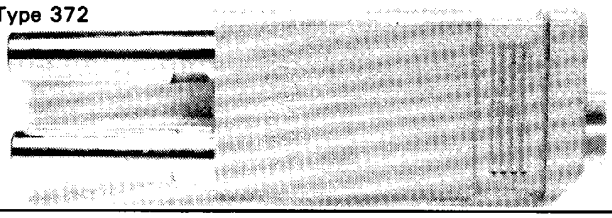
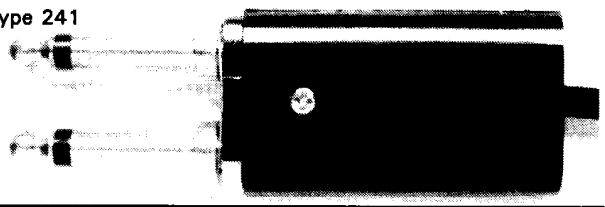
Equipment	Critical Specifications	Application	Recommended -hp- Model No.
75Ω to balanced 124Ω matching pad, consisting of:		P	
10ΩResistor	1%		0757-0346
20Ω Resistor	1%		0757-0384
121Ω Resistor	1%		0757-0403
68.1Ω Resistor	1%		0757-0397
20Ω Ten-Turn Potentiometer			2100-3315
200Ω Ten-Turn Potentiometer			2100-3095
2kΩ Ten-Turn Potentiometer			2100-3109
1kΩ Ten-Turn Potentiometer			2100-3154
Enclosure	Three (f) BNC, grounded		Pomona 3232
75Ω to Balanced 135Ω matching pad, consisting of:		P	
24.3Ω Resistor	1%		0757-0386
121Ω Resistor	1%		0757-0403
75Ω Resistor	1%		0757-0398
500Ω Ten-Turn Potentiometer			2100-3123
2kΩ Ten-Turn Potentiometer			2100-3109
1kΩ Ten-Turn Potentiometer			2100-3154
Enclosure	Three (f) BNC, grounded		Pomona 3232
75Ω to balanced 600Ω matching pad consisting of:		P	
10Ω Resistor	1%		0757-0346
619Ω Resistor	1%		0757-0418
110Ω Resistor	1%		0757-0402
10Ω Ten-Turn Potentiometer			2100-3164
10kΩ Ten-Turn Potentiometer			2100-3103
500Ω Ten-Turn Potentiometer			2100-3123
Enclosure	Two (f) BNC, grounded		Pomona 3230
75Ω to balanced 150Ω matching pad consisting of:			
10Ω Resistor	1%		0757-0346
36.5Ω Resistor	1%		0757-0390
110Ω Resistor	1%		0757-0402
82.5Ω Resistor	1%		0757-0399
10Ω Ten-Turn Potentiometer			2100-3164
500Ω Ten-Turn Potentometer			2100-3123
(2) 2kΩ Ten-Turn Potentiometer			2100-3109
Enclosure	Two (f) BNC, isolated		Pomona 3239
Power Combiner Consisting of:	75Ω	P	
(3) 25Ω Resistors	0.1%		0698-8011
Enclosure	Three (f) BNC, grounded		Pomona 3232
124Ω Balance Testing Apparatus, consisting of:		P	
(2) 10Ω Resistors	1%		0757-0346
(2) 62Ω Resistors	0.1%		0698-6800
Enclosure	Three (f) BNC, one (m) BNC, grounded		Pomona 3234
135Ω Balance Testing Apparatus consisting of:		P	
(2) 10Ω Resistors	1%		
(2) 67.3Ω Resistors	0.25%		0757-0346
Enclosure	Three (f) BNC, one (m) BNC, grounded		0698-8558 Pomona 3234
600Ω Balance Testing Apparatus consisting of:			
(2) 10Ω Resistors	1%		0757-0346
(2) 300Ω Resistors	0.1%		0698-6346
Enclosure	Three (f) BNC, isolated		Pomona 2102

Table 8-14. Recommended Test Equipment (Cont'd).

Equipment	Critical Specifications	Application	Recommended -hp- Model No.
150Ω Balance Testing Apparatus, consisting of:		P	
(2) 10Ω Resistors	1%		0757-0346
(2) 75Ω Resistors	0.1%		0698-7363
Enclosure	Three (f) BNC, isolated		Pomona 2102 Available from: Pomona Electronics P.O. Box 2767 Pomona, CA 91766
600Ω Feedthrough, consisting of:			
600Ω Resistor	0.1%		0698-7408
Connector	BNC		1250-0052
Connector	BNC		11048-27603
Connector	BNC		1250-0083
Threaded Sleeve	BNC		11048-27604
(3) 75Ω BNC Coaxial Cables	3'	P	11652-60014
(2) 75Ω BNC Coaxial Cables	2'	P	11652-60013
(3) 75Ω BNC Coaxial Cables	1'	P	11652-60012
(3) 50Ω BNC Coaxial Cables	1'	P	11170A
Siemens 3-prong to (m) BNC Cable (must be modified, see Table 4-4) (3586A only)*		P,A,R	W & G, k164
Siemens 1.6/5.6mm to (f) BNC Adapter (3586A opt 001 only)*		P,A,R	W & G, s230 Available from: W & G Instruments Inc. 119 Naylon Ave. Livingston, NJ 07039
(2) (m) BNC to single Banana jack adapter		P	Pomona 3430-0
(3) Mini-Weco to (f) BNC adapter (3586B standard)*		P	1250-0556
(3) Large-Weco to (f) BNC adapter (3586B opt. 001)*		P	1250-0591
(2) 1/4" Phone Plug to (f) BNC adapter (3586B)*		P	1251-3759
Weco 310 plug to (f) BNC adapter (3586B)*		P	1251-3757
Dual Banana to (f) BNC adapter (3586C)		P	1251-2277
(2) BNC "T"		P	1250-0781
(m) BNC to (m) BNC adapter		P	1250-0216
75Ω Resistor	0.1%	P	0698-7363
50Ω Resistor	0.1%	P	0699-0064

*See Table 8-15

Table 8-15

ADAPTER DESC.		
Siemans 3-prong to (M) BNC Cable (must be modified)	Siemans 3-Prong 	Available From: W&G Instruments, Inc., 119 Naylon Avenue, Livingston, N.J. 07039
Siemans 1.6/5.6mm to (F) BNC Adapter	Siemans 1.6/5.6mm Model S230 	Available From: W&G Instruments, Inc. 119 Naylon Avenue, Livingston, N.J. 07039
Mini-Weco to (F) BNC Adapter	(2) WECO Type 440 or 	WECO Type 440 -hp- P/N 1250-0556
	(1) WECO Type 443 	WECO Type 443 Available From: Trompeter Electronics 8936 Comanche Ave., Chatsworth, CA. 91311
Large-Weco to (F) BNC Adapter	(2) WECO Type 358 or 	WECO Type 358 -hp- P/N 1250-0591
	(1) WECO Type 372 	WECO Type 372 Available From: Trompeter Electronics 8936 Comanche Ave., Chatsworth, CA. 91311
¼" Phone Plug to (F) BNC Adapter	(2) WECO Type 347 or 	WECO Type 347 -hp- P/N 1251-3759
	(1) WECO Type 241 	WECO Type 241 Available From: Pomona Electronics, 1500 East Ninth St., Pomona, CA. 91766
WECO 310 Plug to (F) BNC Adapter	WECO Type 310 	-hp- P/N 1251-3757

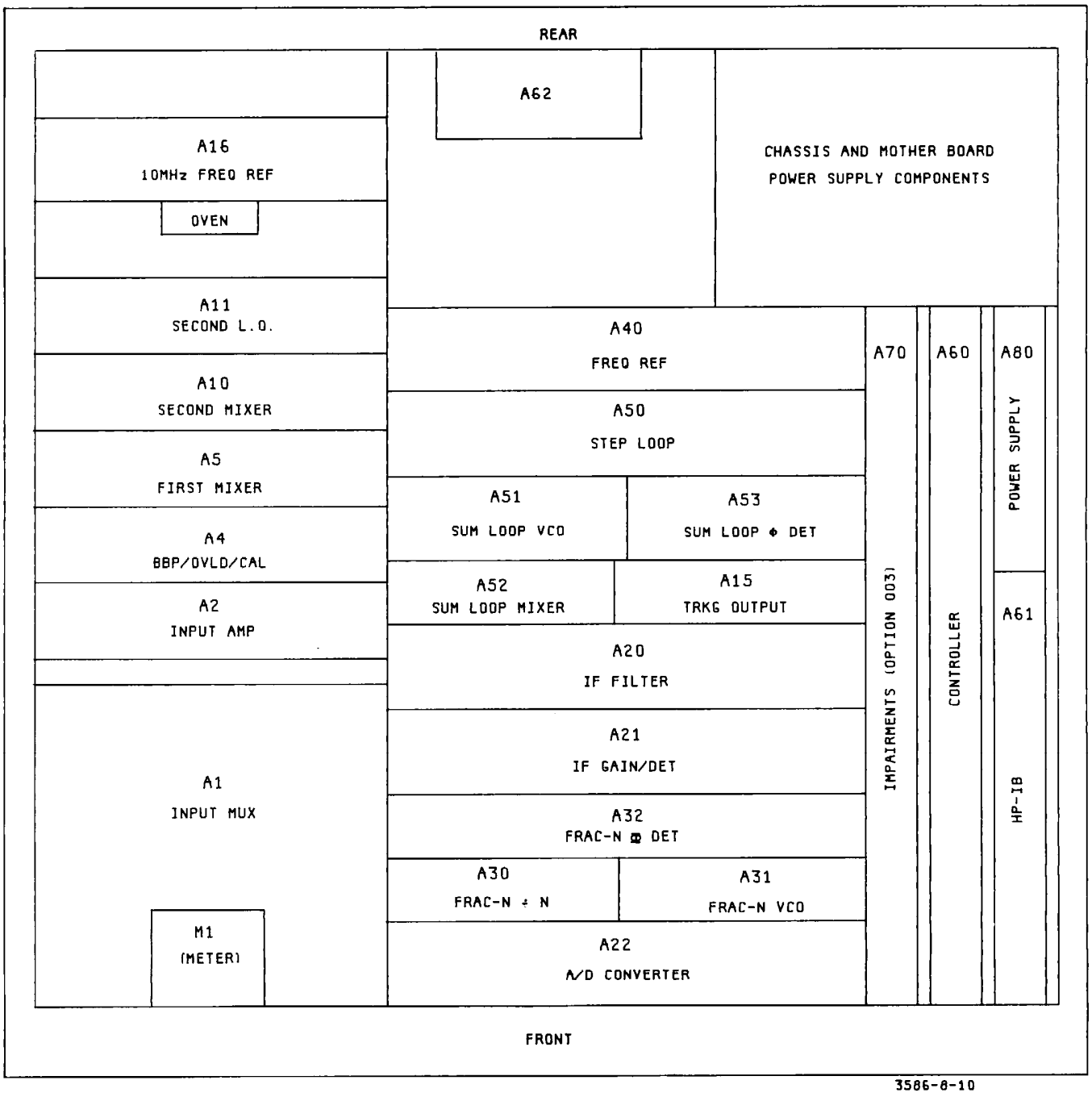


Figure 8-11. Printed Circuit Board Layout.

Table of Contents

INPUT
SERVICE GROUP A

8-A-1. ADJUSTMENTS (CROSS REFERENCE).

8-A-2. Input Multiplexer Adjustments (A1).

Designation	3586 Model	Adjustment Title	Paragraph
A1C2	A/B/C	Calibration Return Loss	5-17 (b)
A1C4	C	50Ω Return Loss	5-17 (b)
A1C10	B	Balance	5-18
A1C22	A/B/C	600Ω Response	5-18
A1L1	A/B/C	75Ω Return Loss	5-17 (b)
A1L2	C	75Ω Return Loss	5-17 (b)
A1L12	A/B	150Ω Response	5-18
A1L13	B	150Ω Return Loss	5-18
A1R15	A/B	150Ω Gain	5-18
A1R28	C	600Ω Gain	5-18

8-A-3. Input Amplifier Adjustments (A2).

Designation	Adjustment Title	Paragraph
A2C4	20dB Attenuation Adjust	5-17 (c)
A2C5	40dB Attenuation Adjust	5-17 (c)
A2C7	Return Loss Compensation	5-17 (b)
A2C32	Flatness Adjust	5-17 (c)
A2C33	Flatness Adjust	5-17 (c)
A2R5	40dB Attenuation Adjust	5-17 (c)
A2R12	Distortion Adjust	5-19
A2R105	Regulator Adjust (±10.5V)	5-17 (a)

8-A-4. Input Mixer Adjustments (A5).

Designation	Adjustment Title	Paragraph
A5C23	Notch Adjust	5-14
A5C53,56, 59,63,65	Flatness Adjustments	5-13
A5C61	50MHz Adjust	5-12
A5L21	Bandpass Slope	5-14
A5L25	50MHz Adjust	5-14
A5R4	Limiter Balance	5-16
A5R24	Flatness Adjust	5-14
A5R50	Bandpass Ripple	5-13

8-A-5. THEORY OF OPERATION (CROSS REFERENCE).

8-A-6. Input Multiplexer (A1) - Paragraph 8-119.

8-A-7. Input Amplifier (A2) - 8-124.

8-A-8. Input Mixer (A5) - 8-132.

8-A-9. TROUBLESHOOTING DATA.

8-A-10. Signal flow through the input section is quite straightforward, and conventional signal tracing methods may be used.

8-A-11. Input Multiplexer (A1) Troubleshooting.

8-A-12. The input multiplexer performs input impedance and voltage level conversions in accordance with Table 8-A-1. Note that a given input power level (e.g. 0dBm) will produce the same voltage at A1J1 regardless of which input port is used. The only exception to this is when using the 3586C 50Ω input, at which time the output will be 1.78dB lower than when using other inputs. (This correction factor is added later by the processor.)

Table 8-A-1. Input Multiplexer (A1) Voltage Levels and Relay Configurations.

Model	Input Termination	Input Voltage at 0dBm	A1 Relays Activated	Output Voltage (A1J1)
3586A	75Ω unbalanced	.275 Vrms	K2, K3	.275 Vrms
	10kΩ || 50pF	.275	K2	.275
	150Ω balanced	.387	K1, K2	.275
	600Ω balanced	.775	K1, K2, K4	.275
	600Ω balanced (bridged)	.775	K1, K2, K4, K5	.275
3586B	75Ω unbalanced	.275 Vrms	K2, K3	.275 Vrms
	10kΩ || 50pF	.275	K2	.275
	124Ω balanced	.352	K1, K2	.275
	135Ω balanced	.367	K1, K2	.275
	600Ω balanced	.775	K1, K2, K4	.275
	600Ω balanced (bridged)	.775	K1, K2, K4, K5	.275
3586C	50Ω unbalanced	.224 Vrms	K2, K3, K4	.224 Vrms
	10kΩ || 50pF	.224	K2	.224
	75Ω unbalanced	.275	K2, K3	.275
	10kΩ || 50pF	.275	K2	.275
	600Ω balanced	.775	K1, K2	.275
	600Ω balanced (bridged)	.775	K1, K2, K5	.275

8-A-13. The input multiplexer is the only part of the signal path for which the instrument does not produce and use internal calibration factors. Any deviations from flat frequency response here will show up as measurement errors.

8-A-14. Input Amplifier (A2) Troubleshooting.

8-A-15. The Input Amplifier operates at one of twelve different gains, as determined by the controller. Proper gain may be verified in accordance with Table 8-A-2 by applying a known signal to A2J1, either directly or through input multiplexer A1, and measuring the output at A2J3 with an oscilloscope or voltmeter.

8-A-16. TF7, TF13 (see paragraph 8-81) and AUTO-CAL each provide quick verification that all 12 levels of RF gain are operating correctly. The full scale ENTRY mode may be used to select a specific gain step for troubleshooting purposes (see Table 8-A-2).

8-A-17. The frequency response of A2 and following stages need not be perfectly flat, as the AUTO-CAL circuits will measure and compensate for deviations of up to ±3dB. However, CAL errors (see paragraph 8-38) will occur any time a computed correction factor exceeds 3dB.

8-A-18. Relay A2K1 is activated during AUTO-CAL to disconnect the input signal and inject instead the calibration source from A4. This source is an accurate −40dBm signal (−20dBm for Full Scale settings greater than ØdBm) at the frequency to which the 3586A/B/C is tuned. Any problem here will cause all calibration, TF7 or TF13 steps to fail.

Table 8-A-2. Input Amplifier (A2) RF Gain Steps.

TF13 Step	TF7 Step	CAL Error (CE-N)	Full Scale	Attenuation Value	K2	K3	Amplification Value	K4	Q7	Total Gain (Amplification) 3586A/B	3586C
1.0	rF00	N=0	+20dBm	−40dB	0	1	+ 6dB	0	1	−34dB (.020)	−39dB (.011)
1.1	rF01	1	+15	−40	0	1	+11	0	0	−29 (.036)	−34 (.020)
1.2	rF02	2	+10	−40	0	1	+16	1	1	−24 (.063)	−29 (.036)
1.3	rF03	3	+ 5	−40	0	1	+21	1	0	−19 (.11)	−24 (.063)
1.4	rF04	4	0	−20	0	0	+ 6	0	1	−14 (.20)	−19 (.11)
1.5	rF05	5	− 5	−20	0	0	+11	0	0	− 9 (.36)	−14 (.20)
1.6	rF06	6	−10	−20	0	0	+16	1	1	− 4 (.63)	− 9 (.36)
1.7	rF07	7	−15	−20	0	0	+21	1	0	+ 1 (1.1)	− 4 (.63)
1.8	rF08	8	−20	0	1	0	+ 6	0	1	+ 6 (2.0)	+ 1 (1.1)
1.9	rF09	9	−25	0	1	0	+11	0	0	+11 (3.6)	+ 6 (2.0)
1.10	rF10	A	−30	0	1	0	+16	1	1	+16 (6.3)	+11 (3.6)
1.11	rF11	b	−35	0	1	0	+21	1	0	+21 (11)	+16 (6.3)

NOTES:

1. For TF Definition see paragraph 8-49.
2. 1 = ON or energized.
   0 = OFF or de-energized.
3. Amplification in 3586C will be 5dB less.
4. Use LOw DISTortion mode and 100dB range.
5. Number in ( ) is the voltage amplification factor. For example: with a total gain on A2 of +6dB, an input signal at A2J1 of 275mVRMS (0dBm into 75 ohms) would be 550mVRMS at A2J3 (275x2.0).

8-A-19. Input Mixer (A5) Troubleshooting.

8-A-20. The Input Mixer further buffers and filters the input signal prior to mixing it with the first Local Oscillator (L.O.). The negative lead of A5C76 provides a convenient test point for observing the process signal just prior to its entering the mixer transformer A5T20. When doing so, the lead may be pulled from its socket for connection to an oscilloscope, spectrum analyzer, etc. Look for an exact duplication of all input signals below 32.5MHz at levels never exceeding 30mV p-p (−19dBm, 75Ω).

8-A-21. The first L.O. drive to mixer transformer T3 is about 2.0Vp-p and will usually be at a frequency 50MHz higher than the frequency to which the 3586A/B/C is tuned.

8-A-22. *Measurement of any First L.O. or First I.F. signal requires proper use of a high impedance (X 10 or FET input) probe, maintaining short, direct grounds at all times.*

8-A-23. A quick verification of the Input Mixer may be performed in the following manner: Place A5 on an extender board. Apply a 1MHz signal to the 3586A/B/C input section by activating TF12 (see paragraph 8-79). Connect an oscilloscope or spectrum analyzer to XA5 (A2). As the 3586A/B/C is tuned from 950kHz to 1050kHz, observe constant 40mVp-p (−17dBm, 75Ω) output between 995 and 1005kHz, decreasing to very low levels at 15kHz or more away from 1MHz. The A5 output frequency will be 50MHz ±50kHz as seen on the spectrum analyzer for XA5 (A2).

8-A-24. INPUT SECTION PROBLEMS.

8-A-25. Amplitude Accuracy Problems.

8-A-26. Carefully follow the problem isolation techniques described in Table 8-9 (Troubleshooting Hints) under "Amplitude Measurements Incorrect" to help determine the faulty stage(s). Using the functional block diagram (Figure 8-A-7) and the general troubleshooting data (paragraph 8-A-9), trace a known input signal through the stages until the problem area is found. The following hints may also be of value.

8-A-27. A1 Amplitude Problems. Frequency response of this assembly is critical. Be prepared to verify all A1 adjustments if any components are changed or wires moved. AUTO-CAL will not correct for any inaccuracies in A1 frequency response. **Deviations from a perfectly flat response will show up as measurement errors!**

8-A-28. A1 can always be bypassed by inputting a signal from a 75 ohm source directly into A2J1. (Remember to supply a 75 ohm termination or subtract 6dB from all readings.)

8-A-29. A2 Amplitude Problems. Troubleshooting the input amplifier should be fairly straightforward, using the functional block diagram and Table 8-A-2. The various gain levels can be set by using the Full Scale ENTRY mode, (Range 100dB) or by shorting to ground the appropriate relay control line. Under normal conditions, the AUTO-CAL cycle will detect and compensate for overall gain errors of up to ±3dB.

8-A-30. A5 Amplitude Errors. The input mixer operates at a fixed gain. If an input signal is less than the current full scale value, then the signal levels shown on the functional block diagram should be lowered in proportion (this does not apply to the First Local Oscillator signal which should always remain at the same level).

8-A-31. The adjustments in the 32.5MHz Low Pass Filter are critical and interactive as are those in the 50MHz IF Filter. Adjustment should only be made when absolutely necessary, and strictly in accordance with the appropriate procedure.

8-A-32. Overall gain of the input mixer can be lowered due to insufficient First L.O. drive. Verify the proper signal levels at A5T3.

8-A-33. Calibration Errors.

8-A-34. Failures displayed as CE-N where N = Ø,1,2...9,A,b indicate an amplitude error of greater than 3dB at the current operating frequency. They should be traced as described above.

8-A-35. Failures displayed during Test Function 13 (e.g. FAIL 4 16) do not necessarily indicate a unit failure. (The limits for this confidence check are ±2dB, while the 3586A/B/C can self-compensate for errors of up to ±3dB). Note the readings taken during this portion of TF13. If they are within the range −20 ± 3dBm or −40 ± 3dBm, then the AUTO-CAL should work. If it does, and there are no Calibration failures (CE-N), then the instrument may be used with reasonable confidence. It should always be remembered, however, that the calibration cycle can pass even though the First L.O. frequency is incorrect. See Table 8-9. under "Frequency Measurements Incorrect" (Steps 3-5) for more information on First L.O. problems.

8-A-36. Distortion Problems - Harmonic and Intermodulation.

8-A-37. Distortion is an abnormal condition occurring within the RF and IF stages of the 3586A/B/C, which causes signals to appear within the instrument at frequencies for which no input has been applied.

8-A-38. Harmonic distortion (HD) is occurring when the various harmonics of a pure input signal are found within the instrument at their appropriate frequencies. Refer to the HD Performance Test in Volume I of the Service Manual for procedures to measure HD.

8-A-39. Intermodulation distortion (IMD) is occurring when two pure signals (f_1 and f_2) at the input are observed to "mix" and produce additional signals at $f_1 + f_2$ and $f_1 - f_2$ (second order IMD). The same conditions that cause second order IMD may generate harmonics of the input signals, which will also mix causing third and higher order IMD to appear at frequencies such as $2f_1 - f_2$, $2f_2 - f_1$, $2f_2 - 2f_1$, etc. Refer to the IMD Performance Test in Volume I of the Service Manual for procedures to measure IMD.

8-A-40. The importance of having pure input signal(s) cannot be over-stressed. Distortion caused by the test set up will generally be indistinguishable from distortion caused within the instrument. This can make it impossible to obtain accurate performance measurements. It is best to verify the test set up independently, prior to use, using a high quality spectrum analyzer.

8-A-41. Harmonic distortion can occur anywhere in the analog signal path from the input jack up to the input mixer on A5. Intermodulation distortion can occur anywhere up to the IF detection circuitry on A21. Troubleshooting methods for either type of distortion are generally the same and involve isolating the source of the distortion to a particular stage.

8-A-42. Troubleshooting is easiest with a spectrum analyzer. Observe the spectrum at various points along the signal path from A1 to A2 to A5 (and into Service Group B if necessary). If the distortion is being created within the instrument, it will appear first at test points in the offending stage.

8-A-43. Without a spectrum analyzer, the distortion source can still be isolated, using the procedures described in the following paragraphs.

8-A-44. Isolating Distortion to a PC Board.

8-A-45. First, determine the extent of the problem. For HD, tune the 3586 to the second through at least the fifth harmonic of the input signal(s). HD exists when the amplitude measurement is greater than 70dB below Full Scale for any harmonic of a pure input. Next, for IMD, tune the 3586 to at least the following frequencies. For inputs of f_1 and f_2, measure the amplitude of $f_1 + f_2$, $f_1 - f_2$, $2f_1 - f_2$, and $2f_2 - f_1$. This will cover all second and third order IMD products and give you an idea of what you have to get rid of, to cure the problem. IMD should also be <70dB below Full Scale.

8-A-46. Next, determine if the distortion occurs for all input impedances (when trying this it is not necessary to use 124Ω, 135Ω, 600Ω, etc. sources -- just vary the source amplitude appropriately to obtain the same displayed measurement reading). If failure only occurs for a single input impedance, troubleshoot that part of the input multiplexer A1.

8-A-47. If the distortion is there for all input impedances, isolate the board that is causing the problem as follows:

1. Leaving all instrument settings unchanged, hook the input signal(s) directly into A2J1. (Use the A15J2 black coax from the rear panel BNC labeled "F_o (0-32MHz)" to make the connection to A2J1, if an appropriate adapter is not available.) If the distortion is now missing, the problem is on A1. Proceed to paragraph 8-A-50 for further isolation.

2. Attenuate the input signal(s) to −18dBm total power. (If the test is for intermodulation distortion, each input signal should be half the total, or −21dBm). Apply to A5J1 using the A40J1 red coax from the rear panel BNC labeled "INPUT-EXT REF" or an appropriate adapter cable. If the distortion products are now missing, the problem is on A2. Proceed to paragraph 8-A-51 for further isolation.

3. If the distortion is still present and it is HD only, or HD **and** IMD, the problem should be on A5. If IMD **only** is present, the problem might still be past A5. Proceed to paragraph 8-A-53 to isolate the problem further.

8-A-48. Isolating Distortion on A1, A2, or A5.

8-A-49. Once the distortion has been isolated to a specific PC board (A1, A2, or A5) using the procedures found under paragraph 8-A-44, further isolation may be possible using the following information.

8-A-50. Distortion Within A1. The input multiplexer is an unlikely source for distortion, as it contains no active circuitry within the signal path. When isolating to a particular input impedance path, remember that relay contacts may fail, remaining either always open or always shorted. As a general rule, distortion within A1 (or in any stage, for that matter) will be caused by some component (or group of components) operating in a non-linear fashion.

Examples of this include saturating inductors (cracked cores) or leaky capacitors as well as active components such as transistors, diodes, etc.

8-A-51. Distortion Within A2. A common cause of distortion in the input amplifier is overdriving. Verify proper signal levels at all test points, and proper operation of the gain switching logic. Check also the DC bias voltages in the amplifier stages.

8-A-52. To determine whether the distortion is being caused by the RF amplifier (Q1-Q6) or buffer stages (Q10-Q14) perform the following steps:

1. Tune to, and record, the amplitude of the distortion product.

2. Apply a short from A2Q7(E) to ground, lowering the RF amplifier gain by 5dB. Observe the new display measurement reading.

3. If the distortion is being caused within or prior to the RF amplifier, the amount of distortion will also drop 5dB.

4. If the distortion remains the same, it's source (if within A2) is in one of the buffer stages.

8-A-53. Distortion Within A5. Again, check signal levels and bias voltages throughout. If the problem is harmonic distortion, the cause will be somewhere prior to T20. Intermodulation distortion can occur anywhere on this board (or further down the signal path in Service Group B), subject to the following test:

1. Measure second and third order IMD for frequency **separations** of both 200Hz and 1MHz (e.g. signals at 99,800Hz and 100,000Hz represent a separation of 200Hz).

2. If both tests fail, the problem is prior to the crystal filter.

3. If only the 200Hz separation test fails, the problem is within the crystal filter or the 14dB amplifier or not on A5. (Remember that A5Y1 and Y2 are a matched set and must be replaced together). Further isolation to prove whether A5 is good requires a Spectrum Analyzer. Refer to the IMD discussion in Service Group B.

8-A-54. Distortion within the A5 mixing circuits can occur due to a low signal level in the First Local Oscillator drive. The L.O. imput to diode mixer A5CR1 must be pure, balanced, and of correct amplitude. Be sure to check it carefully as shown on Figure 8-A-7.

8-A-55. Noise Floor Problems.

8-A-56. A noise problem exists when the displayed reading exceeds that specified in Table 8-1. If the high reading is fairly constant from 50Hz to 32.5MHz, then the problem is truly a noise problem. If the high reading only exists at certain frequencies or frequency bands, then the problem is most likely spurious signals (see the information on spurs under "High Noise Floor" in Table 8-9). Because spurs are far more likely to occur than excessive true broadband noise, it is recommended that the service technician first verify (and correct, if necessary) the performance of the instrument with respect to residual spurious signals (paragraph 4-37).

8-A-57. If the problem appears to be solely a noise problem, the techniques listed in Table 8-9 under "High Noise Floor" should be followed to isolate the trouble to a particular PC board. Following are some hints for further isolation of a noise problem:

1. Remember that isolation to a board doesn't necessarily mean that noise is being generated by that board -- the source may be external, but could be being picked up by that stage due to shielding problems.

2. Trace the noise, using a spectrum analyzer, from point-to-point on the board to discern where it may begin.

3. In a variable gain stage such as A2, change the gain by grounding relay control lines to see if the noise level changes. Whether or not the noise level changes will indicate if the noise is before or after the amplifier.

4. The most probable source of wideband noise within the input stages is a single marginal component (active or passive) in the analog signal path.

8-A-58. Return Loss and Balance Problems.

8-A-59. The only boards that can affect return loss and balance performance are A1 and A2. A simple test (paragraph 8-A-67) isolates the cause of the problem to a single board.

8-A-60. **Return loss** is a measure of the accuracy of a port's input impedance, e.g. does the 600 ohm input jack exactly represent a 600 ohm load impedance at all frequencies? (Remember, this is an AC impedance which is generally not measureable with an ohmmeter.)

8-A-61. **Balance** is a measure of how well the instrument is capable of rejecting a common mode input, that is, a signal that appears simultaneously and in phase at both input terminals. As the name suggests, balance problems are usually caused by some sort of non-symmetrical condition existing with respect to ground, somewhere before the balanced to unbalanced conversion (balun).

8-A-62. For balance and return loss problems, determine first whether the problem exists for all inputs or just certain ones, and whether it is frequency related. The magnitude of the error will suggest whether the problem is merely misalignment of A1 (small error) or if component failure has occurred (large error).

8-A-63. Failures that occur only at low frequencies probably indicate a failed component such as one of the transformers or coupling capacitors.

8-A-64. Failures that occur only at high frequencies probably indicate misadjustment of a variable capacitor or inductor. (See paragraph 8-A-1.)

8-A-65. Failures that occur at all frequencies again indicate component failure. Check relay contacts, cabling, resistor values, etc.

8-A-66. Failures that occur for all input impedances are probably caused by a problem "downstream" from A1K1. Failures that occur for only certain input impedances may be isolated using the schematic and Table 8-A-1.

8-A-67. If the failure occurs for all input impedances, activate TF2 (paragraph 8-58), thereby de-energizing A1K2. If the problem disappears, component failure or misadjustment is indicated somewhere between A1K2 and A2C10, including cable W14. If the problem remains, it is definitely on A1.

8-A-68. Connectors and Impedances.

8-A-69. Testing all inputs of a 3586A/B/C normally requires a signal source with selectable output impedances (or a collection of matching pads) and a diverse group of interconnecting cable types. For the service facility that is not so equipped, the following information will provide some short cuts.

8-A-70. Using A Standard Source Impedance. For most troubleshooting work, a standard 50 or 75 ohm source may be used to drive any input, providing a correction factor is added to the displayed reading. These factors are listed in Table 8-A-3. For example, consider a signal source with 50 ohms output impedance set for +10dBm output. When connected to the 600 ohm input of a 3586A/B/C, the displayed reading should be +4.53dBm. From the table, it is seen that a correction factor of +5.47dB must be added, which results in the correct reading of +10dBm.

Table 8-A-3. Impedance Mismatch Loss Factors.

Source Impedance	Load Impedance	Correction Factor (Add to displayed reading)
50Ω	75Ω	.18dB
50Ω	124Ω	.87dB
50Ω	135Ω	1.03dB
50Ω	150Ω	1.25dB
50Ω	600Ω	5.47dB
50Ω	900Ω	7.00dB
75Ω	50Ω	.18dB
75Ω	124Ω	.27dB
75Ω	135Ω	.37dB
75Ω	150Ω	.51dB
75Ω	600Ω	4.03dB
75Ω	900Ω	5.47dB

8-A-71. Connector Adapters. In many cases, adapters are available to allow use of standard, BNC equipped coaxial cables for instrument hookup. These are detailed in Table 8-A-4.

8-A-72. Unbalanced Source - Balanced Input. For troubleshooting, an unbalanced source may be used to drive the balanced inputs of the 3586A/B/C. Use the center conductor and shield of the unbalanced source as the two input leads to the instrument. (See Figure 8-A-1).

8-A-73. The above methods will provide useable inputs for signal tracing purposes. They are not, however, rigidly correct, and may show accuracy degradation at high frequencies or low signal levels.

8-A-74. Frequencies vs. Input Impedances.

8-A-75. Each input termination impedance has a different "allowable" frequency input range and the performance specification is defined for that range only. When troubleshooting, be sure to use a proper frequency input signal for the termination impedance you are using. Refer to Table 8-A-5 for allowable frequencies.

Table 8-A-4. Input Connector Adapters.

Model	Option	Input	Connector	Description	BNC Adapter
3586A	Std	75Ω	BNC		None Required
		150Ω	SIEMENS 3 PRONG	9 Rel-6AC	W & G K164
		600Ω	SIEMENS 3 PRONG	9 Rel-6AC	W & G K164
3586A	001	75Ω	SIEMENS 1.6/5.6mm		W & G 5230
		150Ω	SIEMENS 3 PRONG	9 Rel-6AC	W & G K164
		600Ω	SIEMENS 3 PRONG	9 Rel-6AC	W & G K164
3586B	Std	75Ω	WECO 439/440	.300" Video Connector	1250-0556
		124Ω	WECO 443	dual WECO 439/440 0.5 inch spacing	two 1250-0556*
		135Ω	WECO 241	dual 1/4 inch tip-ring Plug 0.63 inch spacing	two 1251-3759*
		600Ω	WECO 310	1/4 inch tip-ring-sleeve Plug	1251-3757
3586B	001	75Ω	WECO 358	.375" Video Connector	1250-0591
		124Ω	WECO 372	dual WECO 358 0.5 inch spacing	two 1250-0591*
		135Ω	WECO 241	dual 1/4 inch tip-ring Plug 0.63 inch spacing	two 1251-3759*
		600Ω	WECO 310	1/4 inch tip-ring-sleeve Plug	1251-3757
3586C	Std	50/75Ω	BNC		None Required
		600Ω	dual banana	0.75 inch spacing	POMONA 1269

*Dual input connectors require a special cable, shown in Figure 8-A-1.

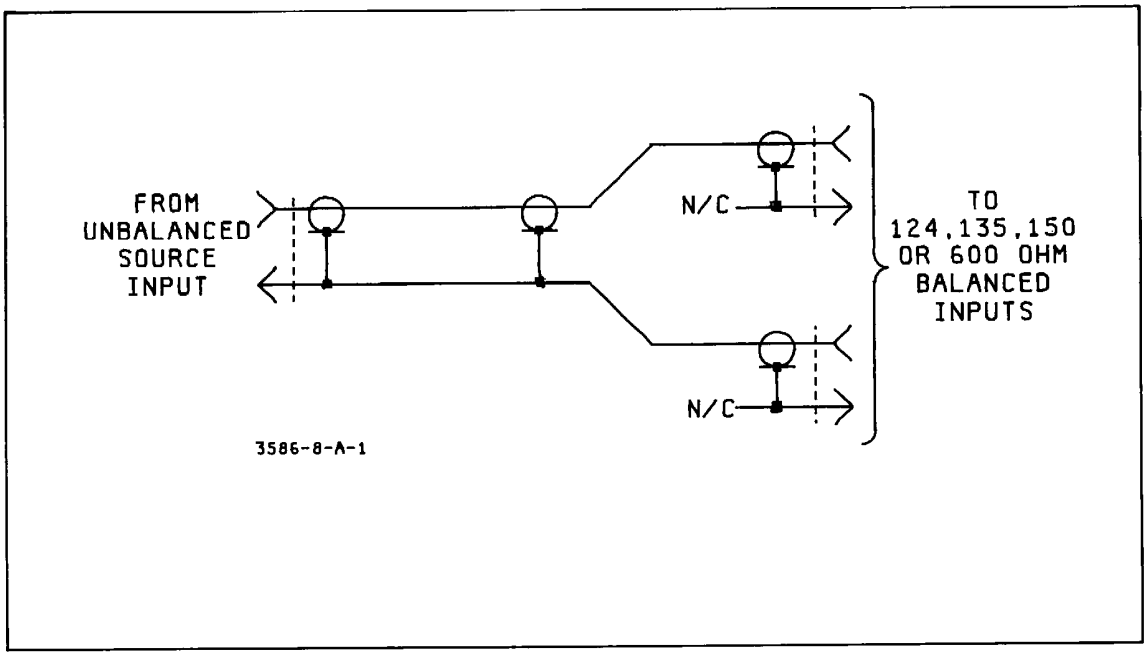


Figure 8-A-1. Unbalanced To Balanced Input Cable.

Table 8-A-5. Frequency Range vs. Input Impedance.

Signal Input Impedance	Frequency Range
75Ω/50Ω/10KΩ (Unbalanced)	200Hz to 32.5MHz
124Ω (Balanced)	4kHz to 10MHz
135Ω/150Ω (Balanced)	4kHz to 1MHz
600Ω/Bridged	100Hz to 108kHz
NOTE *The 124Ω, 135Ω, 150Ω, and 600Ω inputs are useable over wider frequency ranges than specified above.*	

8-A-76. Removal Procedure For Input Multiplexer (A1).

8-A-77. The front panel must be removed first in order to remove A1. Use the following procedure:

1. Turn the instrument off and unplug the line cord.

2. Remove the "beauty strip" along the top front edge of the instrument. The strip simply pulls out.

3. Remove the top cover.

4. Remove the front panel assembly (front panel plus A98 keyboard) by doing the following:

   a. Remove the 8 screws holding the front panel assembly to the instrument. There are four screws along the top front edge of the instrument, and four along the bottom front edge.

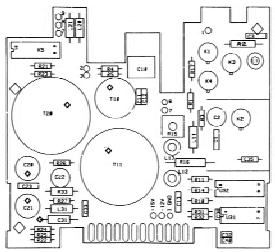
   NOTE

   The 7 short screws (Part No. 0515-0080) go in the 4 top holes and the 3 right-hand holes on the bottom. The single long screw (Part No. 0515-0082) goes in the far left-hand hole along the bottom. These are metric screws.

   b. Slowly pull the front panel assembly out of the instrument about two inches. Then unplug the two cable assemblies attached to the back of the A98 Keyboard. These are the blue ribbon cable between the A98 and A60 controller assemblies, and the brown connector of the cable between the A98 and A99 motherboard.

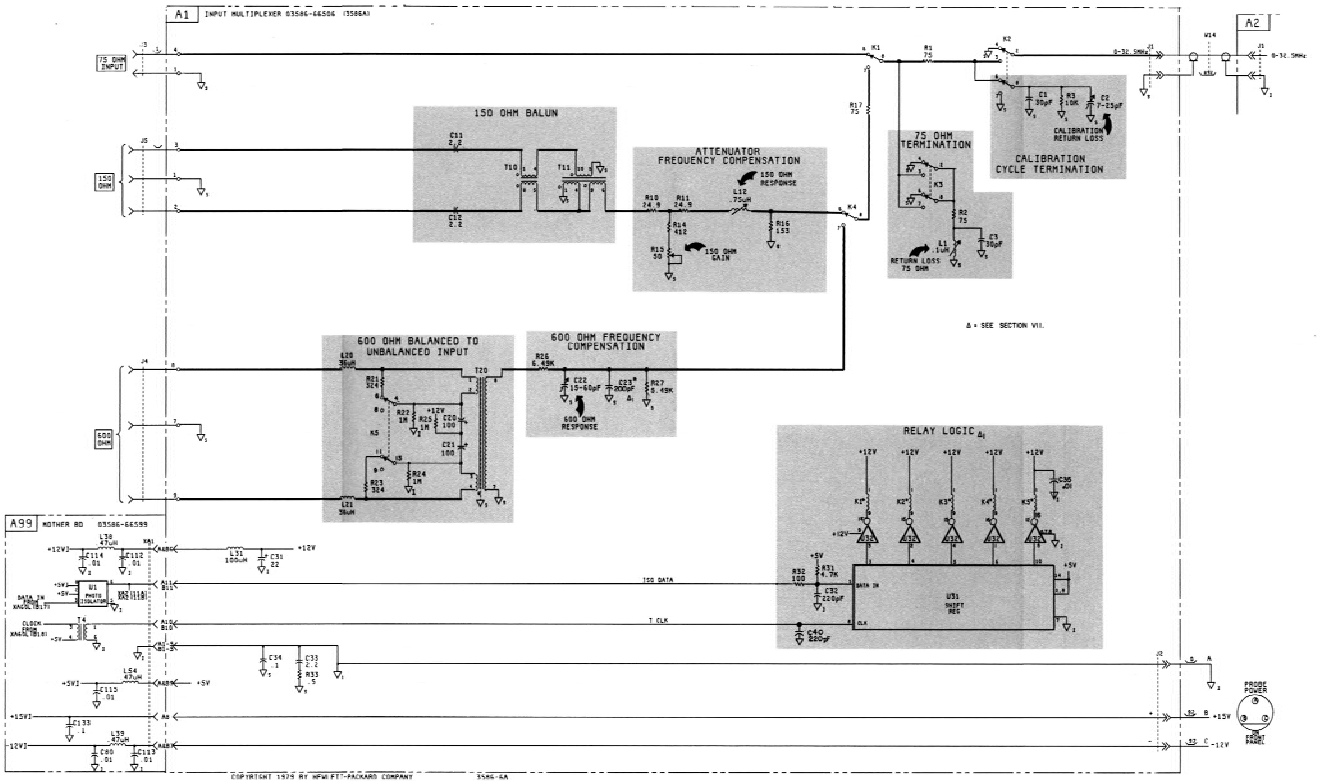
   c. Remove the front panel assembly completely from the instrument. Lay the front panel assembly face down on a surface that won't scratch the front panel.

5. Remove the coaxial cable from the Input Multiplexer A1J1. The entire multiplexer assembly may now be pulled forward and slid out of the instrument.



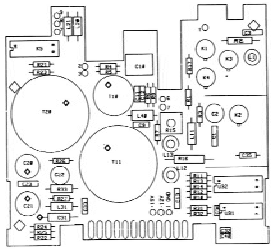
A1
-hp- Part No. 03586-66506
Rev C

NOTES:
1. Isolated ground.
2. Signal ground.
3. See Table 8-A-4 for input connector information.
4. Probe +15VDC is present at probe connector in STANDBY.



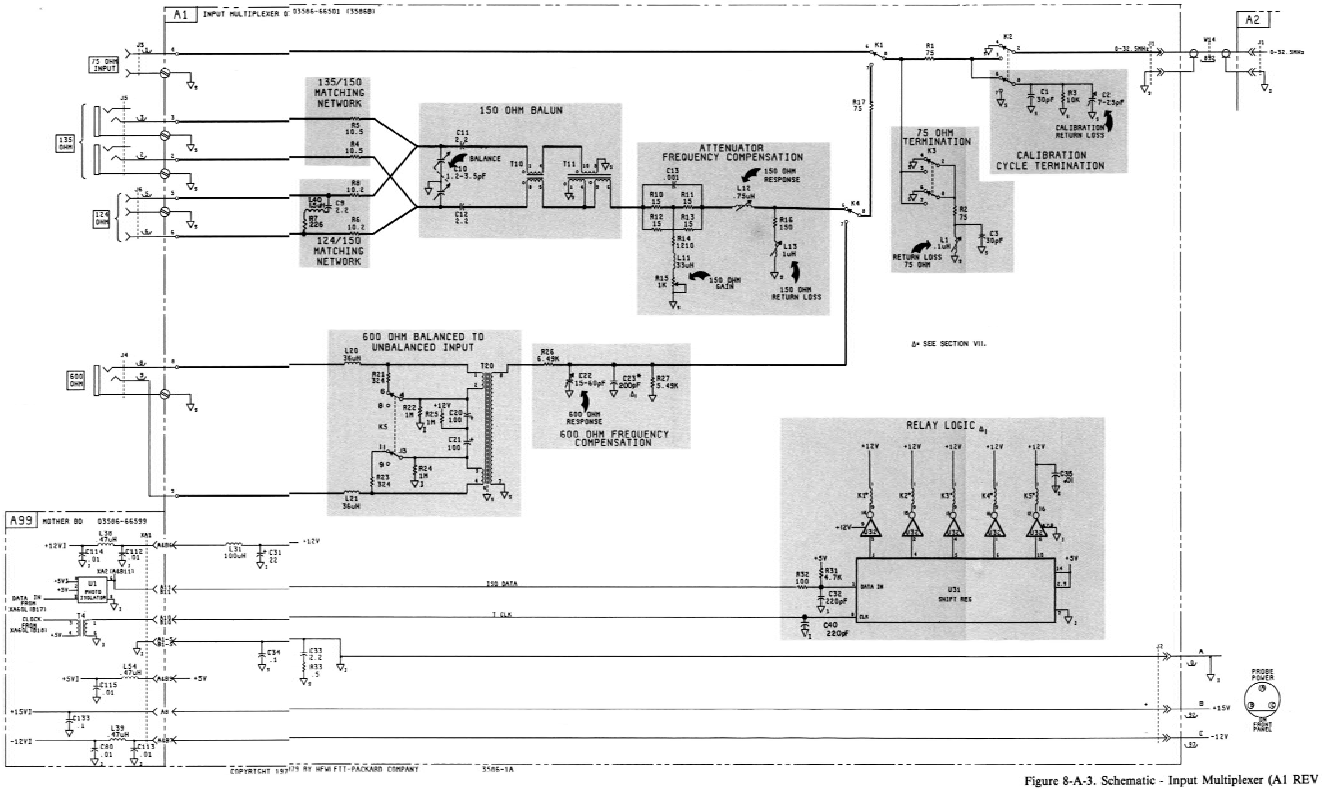
1A

Figure 8-A-2. Schematic - Input Multiplexer (A1 REV C BD) - 3586A



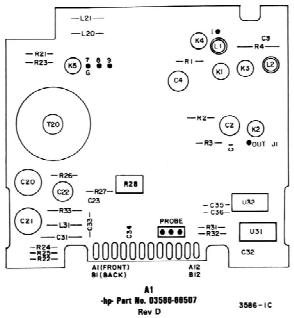
A1
4p- Part No. 03586-66501
Rev C

Notes:
1. Isolated ground.
2. Signal ground.
3. See Table 8-A-4 for input connector information.
4. Probe +15VDC is present at probe connector in STANDBY.



1B

Figure 8-A-3. Schematic - Input Multiplexer (A1 REV C BD) - 3586B



Notes:
1. Isolated ground.
2. Signal ground.
3. See Table 8-A-4 for input connector information.
4. Probe +15VDC is present at probe connector in STANDBY.

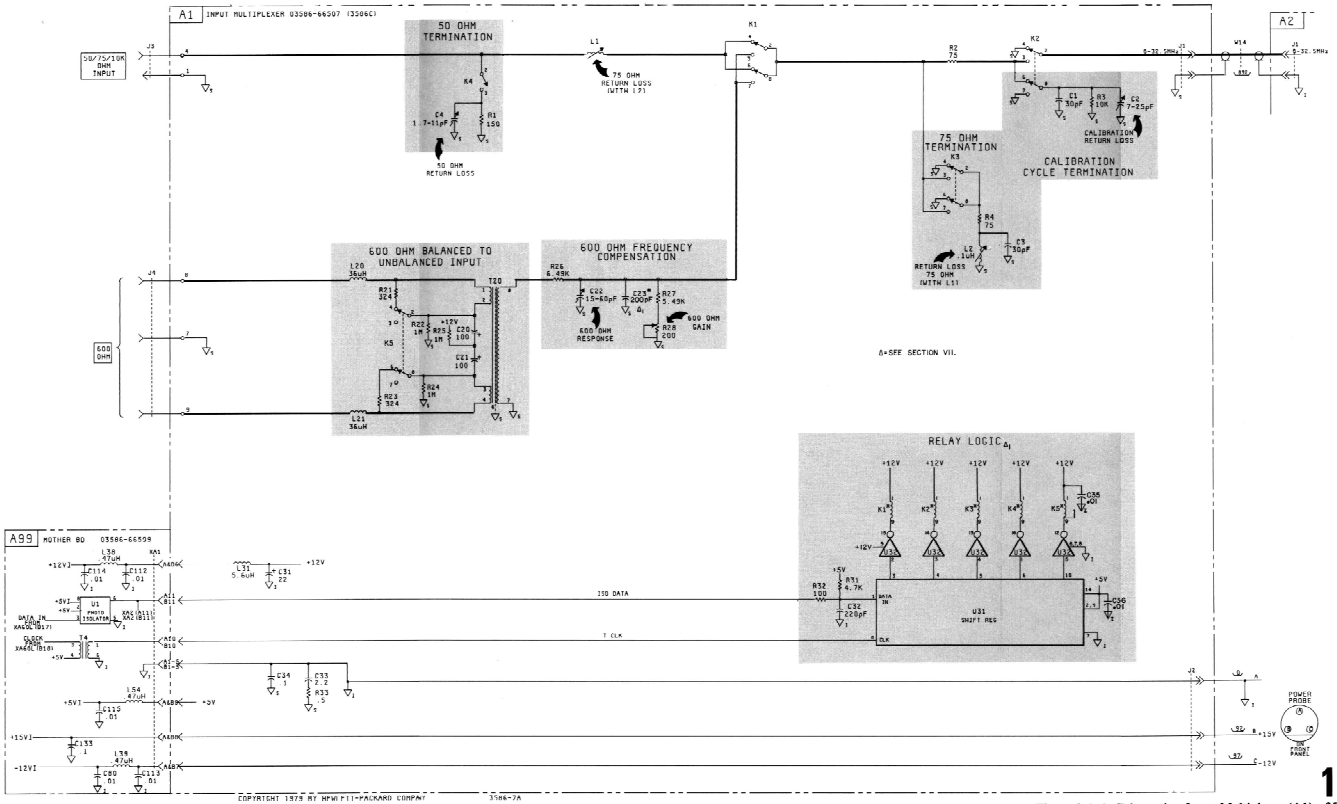


Figure 8-A-4. Schematic - Input Multiplexer (A1) - 3586C

Table of Contents

IF/AUDIO
SERVICE GROUP B

Contents

8-B-1. ADJUSTMENTS (CROSS REFERENCE).

8-B-2. Second Mixer Adjustments (A10).

Designation	Adjustment Title	Paragraph
A10C22	Notch Adjust	5-14
A10L20	Slope Adjust	5-14
A10L24	50MHz Adjust	5-14
A10R43	IF Gain Adjust	5-15
A10L101	14242Hz Adjust	5-10
A10L102	17324Hz Adjust	5-10
A10L103	14400Hz Adjust	5-10
A10L104	16795Hz Adjust	5-10
A10R105	400Hz Bandwidth Gain	5-11

8-B-3. Second Local Oscillator Adjustments (A11).

Designation	Adjustment Title	Paragraph
A11L22	VCO Center	5-7

8-B-4. IF Filter Adjustments (A20).

Designation	Adjustment Title	Paragraph
A20C32, C42	20Hz Filter Adjust	5-10
A20R24	20Hz Gain	5-11
A20R35	20Hz Ripple	5-10
A20R40	20Hz Tilt	5-10
A20L51-L61	2000/3100/1740Hz Filter Adjust	5-10
A20L91-L92	2000/3100/1740Hz Filter Adjust	5-10
A20R95	2000/3100/1740Hz Filter Gain	5-11

8-B-5. IF Gain and Detection Adjustments (A21).

Designation	Adjustment Title	Paragraph
A21R23	10dB Offset	5-9
A21R19	10dB Gain	5-9
A21R25	100dB Offset	5-9
A21R28	100dB Gain	5-9
A21R44	Mixer Balance	5-22
A21R96	Meter ØdB Calibrate	5-9

8-B-6. THEORY OF OPERATION (CROSS REFERENCE).

8-B-7. Second Mixer (A10) - Paragraph 8-137.

8-B-8. Second Local Oscillator (A11) - Paragraph 8-244.

8-B-9. IF Filter (A20) - Paragraph 8-142.

8-B-10. IF Gain/Detection (A21) - Paragraph 8-149.

8-B-11. TROUBLESHOOTING DATA.

8-B-12. Use the IF/Audio function block diagram (Figures 8-B-7, 8) to follow signal paths and levels.

8-B-13. Second Mixer (A10) Troubleshooting.

8-B-14. The Second Mixer filters and amplifies the 50MHz First IF signal prior to mixing it down to the Second IF of 15.625kHz. Following additional amplification, the signal is outputted to the IF Filter Board (A20) at either full (10kHz) bandwidth or through the 400Hz passive bandpass filter.

8-B-15. The Second L.O. drive to mixer transformer A10T2 is about 1.8Vp-p and will be at exactly 49.984375MHz (50MHz-15.625kHz).

8-B-16. *Measurement of the First I.F. or Second L.O. signals requires proper use of a high impedance (x 10 or FET input) probe. Maintain short, direct grounds at all times.*

8-B-17. As a troubleshooting convenience, the 50MHz crystal filter may be bypassed by pulling the appropriate leads of A10R19 and A10C24 from their sockets and placing them in their alternate positions (see schematic, Figure 8-B-1).

8-B-18. Also note that, because the Second I.F. is only 15.625kHz, its level can accurately be measured by most AC voltmeters, freeing the oscilloscope for other observations.

8-B-19. For a quick verification of the 400Hz filter, see paragraph 8-B-23.

8-B-20. IF Filter Troubleshooting (A20).

8-B-21. Note that all signals, upon entering A20, are referenced to PC ground rather than isolated ground. See paragraphs 8-111 to 8-116 for a discussion of 3586A/B/C grounding schemes.

8-B-22. Depending on the control signals to analog switches U3 and U4, the IF signal at TP8 passed through either the 400Hz filter, or the 20Hz filter, or through none at all. From TP8, all signals then travel through the 2000/3100/1740Hz passive bandpass filter.

8-B-23. The 3586A/B/C is capable of internally verifying the performance of its three IF filters. Basically, this is done by activating the internal 1MHz source (RECALL, •, CNTR→FREQ, 7) and manually tuning the instrument through the signal, observing bandwidth, passband ripple, etc. Complete instructions and specifications are found in paragraphs 4-23 through 4-29 in Volume I of the 3586A/B/C Service Manual.

8-B-24. Output amplifier A20U10 provides an additional +25dB of gain at certain full scale settings. Table 8-B-1 provides a comparison of IF gain configurations to full scale settings and test steps.

Table 8-B-1. IF Gain Configurations.

CE-	TF13 Step	TF9 Step	Full Scale Note 3	Full Scale Note 4	U2 (12)	A20U10 Gain	U2 (5)	A21U7 Gain	U4 (15)(16)(19)	A21U8 Gain	Total If Gain	Total If Amplification
	2.0	IF00	+25dBm	+25dBm	1	10dB	1	0dB	1 1 1	0dB	10dB	3.2
b	2.1	01	+20dBm	+20dBm	1	10dB	1	0dB	1 1 0	5dB	15dB	5.6
A	2.2	02	+15dBm	−40dBm	1	10dB	1	0dB	1 0 1	10dB	20dB	10
9	2.3	03	+10dBm	−45dBm	1	10dB	1	0dB	1 0 0	15dB	25dB	18
8	2.4	04	+ 5dBm	−50dBm	1	10dB	1	0dB	0 1 1	20dB	30dB	32
7,3	2.5	05	0dBm	−55dBm	1	10dB	1	0dB	0 1 0	25dB	35dB	56
6,2	2.6	06	− 5dBm	−60dBm	1	10dB	1	0dB	0 0 1	30dB	40dB	100
5,1	2.7	07	−10dBm	−65dBm	1	10dB	1	0dB	0 0 0	35dB	45dB	180
4,0	2.8	08	−15dBm	−70dBm	1	10dB	0	35dB	1 1 0	5dB	50dB	320
		09	−20dBm	−75dBm	1	10dB	0	35dB	1 0 1	10dB	55dB	560
		10	−25dBm	−80dBm	1	10dB	0	35dB	1 0 0	15dB	60dB	1000
		11	−30dBm	−85dBm	1	10dB	0	35dB	0 1 1	20dB	65dB	1800
		12	−35dBm	−90dBm	1	10dB	0	35dB	0 1 0	25dB	70dB	3200
		13	−40dBm	−95dBm	1	10dB	0	35dB	0 0 1	30dB	75dB	5600
		14	−45dBm	−100dBm	1	10dB	0	35dB	0 0 0	35dB	80dB	10000
		15	−105dBm	−105dBm	0	35dB	0	35dB	1 0 0	15dB	85dB	18000
		16	−110dBm	−110dBm	0	35dB	0	35dB	0 1 1	20dB	90dB	32000
		17	−115dBm	−115dBm	0	35dB	0	35dB	0 1 0	25dB	95dB	56000
		18	−120dBm	−120dBm	0	35dB	0	35dB	0 0 1	30dB	100dB	100000
		19			0	35dB	0	35dB	0 0 0	35dB	105dB	180000
		20			1	10dB	0	35dB	1 1 1	0dB	45dB	180
	2.13	21			0	35dB	1	0dB	1 1 1	0dB	35dB	56

NOTES:
1. For TF Definition see paragraph 8-49.
2. 1 = TTL HIGH (> +3.7VDC).
   0 = TTL LOW (< +0.3VDC).
3. USE LOW DISTortion and ENTRY 10.
4. USE LOW DISTortion and AUTO 10, AUTO 100, or ENTRY 100. Full Scale less than −45dBm not selectable in 100dB Range.
5. IF Gain is measured from A20TP9 to A21TP1.

8-B-25. IF Gain/Detection Troubleshooting (A21).

8-B-26. On this board the 15.625kHz IF signal is further processed to provide the following four outputs:

1. Amplified IF signal capable of driving the A22 frequency counter.

2. Detected and logged DC signal for Analog to Digital conversion into a front panel level reading.

3. Demodulated audio to drive the rear panel output jack.

4. Amplified audio to drive the front panel speaker.

8-B-27. IF gain is provided by U7 and U8 according to Table 8-B-1. Total IF gain range is 95dB (70dB on A21 and 25dB on A20), in 5dB steps. Gain can be measured by comparing the amplitudes of A20TP9 and A21TP1. Individual gain steps can be set manually by selecting the appropriate full scale value as shown in Table 8-B-1.

8-B-28. When troubleshooting the DC logger portion of A21, pay close attention to the DC levels, gains and offsets as they all directly affect system accuracy.

8-B-29. Past mixer U13, all signals are in the audio (.3-3.4kHz) range. A single frequency input, such as the 1MHz, 0dBm source used for all signal measurements in this section, will produce an 1850Hz sinewave at TP7. This signal is then routed to the impairments measurement circuitry on A70 (option 003 only) and/or to the audio output amplifier.

8-B-30. The front panel analog meter drive is derived from the signal supplied by A22; a DC voltage which is buffered, corrected and converted to an appropriate current level for the meter movement. This DC voltage is proportional to the "uncorrected" logger output, and must have a calibration factor added to it, the same as is done for the digital display. This correction factor begins as an 8-bit digital word fed to Digital to Analog Converter (DAC) U23, which becomes a DC level and is then added to the meter signal at U20. Table 8-B-2 describes the operation of the correction factor at the DAC. For test purposes, switch A21S2 may be moved to the "T" position. This provides a fixed input voltage to the meter drive circuits which should yield a meter reading of −6.3dB (on the 10dB scale), provided that the correction factors have been zeroed (TF1).

Table 8-B-2. Analog Meter Correction Factors.

Calibration Factor	Digital Input to DAC (U23)	DAC Output U23(4)
−3 dB	01000100	0.0mV
−1 dB	01101100	−100.0mV
− .05dB	01111111	−147.5mV
0 dB	10000000	−150.0mV
+ .05dB	10000001	−152.5mV
+1 dB	10010100	−200.0mV
+3 dB	10111100	−300.0mV

8-B-31. Second L.O. (A11) Troubleshooting.

8-B-32. The Voltage Controlled Crystal Oscillator (VCXO) is the heart of the second L.O. Even with no phase control voltage (U80 pin 6 grounded) it should be capable of providing

proper amplitude drive to the ECL buffers (U33 and U44) at nearly the correct frequency. Having established this, trace the loop back thru U33 to the Mixer (U50), Phase detector (U70) and Integrator (U80), checking for proper signal frequencies, amplitudes and waveshapes.

8-B-33. Error Code E3.1. An error display of E3.1 indicates an out of lock condition on this board. This is caused by the phase control voltage (TP2) to the VCXO being outside the range of +8.8V to −8.8V. Check for proper operation of U70, U80 and U90.

8-B-34. IF/AUDIO SECTION PROBLEM AREAS.

8-B-35. Amplitude and Ranging Problems.

8-B-36. Carefully follow the problem isolation techniques described in Table 8-9 (Troubleshooting Hints) under "Amplitude Measurements Incorrect", "Auto Range Problems", or "Overload/Underload Indications" to help determine the faulty stage(s). Using the functional block diagram (Figures 8-B-7,8) and the general troubleshooting data (paragraph 8-B-11), trace a known input signal through the stages until a problem area is found. The following hints may also be of value.

8-B-37. A10 Amplitude Problems. Signals arriving at the Second Mixer, A10CR1, must be of proper amplitude. Verify proper 2nd L.O. drive level of 1.8Vp-p at T2 primary and secondary. Verify proper signal levels coming from 1st Mixer A5. If the 50MHz crystal filter is defective or mistuned, it can be bypassed by appropriate jumper placement (see paragraph 8-B-17).

8-B-38. Be especially careful when probing near CR1 and U40. A slipped probe here usually means a ruined CR1, which is delicate, static-sensitive, and difficult to replace.

8-B-39. Adjustment of A10R43 (IF Gain Adj) provides a means of compensating for gain variations in the signal path up through U40. If A10R43 is found not to have sufficient range to bring the signal level at the IF test point (IF TP) to 502 mVrms, the problem is very likely in a previous stage. Check all signal levels against the functional block diagram, Figure 8-B-7. Check also for proper instrument set up, proper range, proper full scale selection, proper tuning, etc.

8-B-40. A20 Amplitude Problems. Signal loss through this stage will likely be due to a defective or mistuned filter. These problems are covered in paragraph 8-B-65, "Filter Problems".

8-B-41. It is, however, possible that the 10/35dB IF gain stage (A20U10) may be malfunctioning. Check its operation using the information supplied by Table 8-B-1 and Figure 8-B-7.

8-B-42. A21 Amplitude Problems. First, verify proper programming and operation of the 0/35dB and 0-35dB IF gain stages, using Table 8-B-1.

8-B-43. If the signal level at TP1 is correct, then check the operation of the Logger/Detector circuitry. For proper circuit operation it is important that the signal levels for a given input are correct, but also that their changes for a given variation in input are also correct. For example, verify that all signal levels are correct for a 0dBm, 1MHz input signal with the

3586A/B/C in ENTRY 100 and Full Scale set at 0dBm. Next, lower the input by some number of dB and verify that TP1 lowers by the same number of dB, that TP2 lowers by half that number of dB, and that TP3 drops 10 millivolts for each dB that the input drops.

8-B-44. The signal relationships at TP1, TP2, and TP3 will be as shown in paragraph 8-B-43 for all combinations of 10 or 100dB Range and Full Scale AUTO or ENTRY, although IF gain programming will vary.

8-B-45. If the signal at TP3 is a negative DC level following the above rules, then operation of this part of A21 is probably correct.

8-B-46. Ranging Problems. Range problems (autorange errors, unexpected overload/underload indications) occur when the signal levels arriving at A22 are beyond the range expected for the programmed gain settings. Prior to troubleshooting an OL/UL problem, refer again to Table 8-9 to determine under what conditions OL or UL may normally be expected to appear. Consider the possibility of spurious signals in the RF or IF stages causing "false" autoranging to occur. A quick check in the WIDEBAND mode will reveal the total input power to the instrument. If this level does not match the output power from the source in use, then a spurious signal is probably being generated. This can be a cause of ranging problems.

8-B-47. The vast majority of ranging problems may still be identified by manually stepping from range to range and checking for proper gain, in accordance with Table 8-B-1.

8-B-48. Noise Floor Problems.

8-B-49. These problems may occur anywhere in the RF or IF stages, and the causes will be similar in either case. Refer to paragraph 8-B-55 for a general description of techniques for problem isolation.

8-B-50. For noise that is generated past the IF Test Point (IF TP) on A10, try switching filter bandwidths and noting differences. If the noise goes away when 20Hz is selected, then its source may be in the 400Hz filter or the 400Hz ground isolation amplifier, A20U2. If the opposite applies, then check A20U1.

8-B-51. In cases where the noise seems to originate on A21 or beyond, vary the gains of U7 and U8 to determine whether the noise is also amplified. If the noise originates in or passes through these stages, then its level will also vary.

8-B-52. In order to show up as a measured value, noise will be visible at a fairly high level from A21TP1 onward. If AVEraging affects the amount of noise, then the problem is in or before U5. Finally, if noise fluctuations cannot be seen on the DC level at A21TP3, then the problem probably begins on A22 (Service Group C).

8-B-53. Another cause of noise can be impurities in the Second L.O. signal. Checks at A10TP2 with an oscilloscope or spectrum analyzer may show excessive amplitude modulation or frequency jitter.

8-B-54. Calibration and Self-Test Failures.

8-B-55. Remember again the pass/fail criteria for the various internal tests. Calibration errors (CE-A, b, 9, 8, ... etc.) occur when the measured level of the internal source deviates

from −40dBm or −20dBm (full scale dependent) by more than 3dB. The 3586A/B/C cannot operate accurately when calibration errors occur. TF13 (paragraph 8-81) self-test failures (example, FAIL 2 8) should be looked upon as "early warnings" in most cases, as they allow only a ±2dB variation. During these tests, the actual measured value is displayed, indicating whether the error was acceptable (between 2 and 3dB deviation from the CAL signal), or unacceptable (greater than 3dB).

8-B-56. CE-0 through 9, A, b failure indicates a faulty IF or RF gain step. Use Table 8-B-1 to determine which gain step coincides with which calibration step, then manually select the corresponding full scale value for signal tracing.

8-B-57. CE-C and d indicate errors, respectively, in the 400Hz and 20Hz filters. Refer to paragraph 8-B-65 for filter troubleshooting.

8-B-58. CE-E indicates a failure when using the 100dB range of the detector. Troubleshooting is necessary around A21U5, U9 and U10.

8-B-59. Remember that, for multiple CE failures, the *last* failed step will be the one displayed. Careful observation of the display is necessary to see which other steps fail.

8-B-60. FAIL 2 0 through FAIL 2 11 indicates a specific IF step failure, again indicated in Table 8-B-1. Troubleshoot as described in paragraph 8-B-56.

8-B-61. FAIL 3 1 indicates that the 10dB range of the detector has failed (usually implying that the 100dB range is OK, if nothing else has failed). Again, troubleshoot A21U5, U9 and U10.

8-B-62. TEST 5 - The Audio test should produce reasonably clear, normal volume and musically-pitched audio from the speaker. If it does not, and all other tests have passed, then there is trouble in either the audio portions of A21 (U13 and onward), or the SSB L.O. signal input to U13 is off frequency or missing.

8-B-63. Checking the audio path requires only an oscilloscope or other signal tracer. Verify presence of the audio signal at the output of the product detector, following it off the board to the volume control, back on board to the audio amplifier and, finally, off the board to the speaker. Make sure that switch S1 is correctly set to indicate whether or not the impairments option (A70) is installed. Note that a defective A70 (Service Group G) can cause missing or defective audio. Switching S1 to the "STD" position can eliminate A70 as a possible source of failure.

8-B-64. It is also possible to fail Test 5 because of frequency tuning errors. Correct audio is contingent upon a correctly functioning 1MHz internal reference (from A40), correct First and Second L.O. tuning, and correct USB and LSB oscillator outputs (from A22). Each of these may be individually verified according to information contained in the appropriate service groups (see Figure 8-8).

8-B-65. Filter Problems.

8-B-66. Examine the functional block diagram, Figure 8-B-7, to determine signal flow and switching functions for the filters. Using TF12, each filter can be checked against specifications, using the procedure given in paragraphs 4-23 through 4-29 in Volume I of the 3586A/B/C Service Manual.

8-B-67. The only filter that is not straightforward is the 20Hz crystal filter. Physical damage to any of the crystals or loss of thermal tracking (by the crystals) may cause excessive loss through the filter.

8-B-68. Because all the filters are multi-section, they may be easily checked by observing intermediate test points for signal level. Remember that the center frequency for all filters is 15.625kHz. The best approach to filter troubleshooting is to perform the appropriate adjustment procedure (paragraph 8-B-1) for that filter, noting where problems occur.

8-B-69. Audio Problems.

8-B-70. See paragraph 8-B-62 under TF13 (TEST 5) failures.

8-B-71. Meter problems.

8-B-72. Incorrect readings on the front panel analog meter or the METER output (rear panel) can be traced to A21 or A22. Verify first that the input to A21 is correct. TP4 should be at −.3VDC for a full scale (ØdB) reading, and should drop .1V for every scale division below that. For example, if TP4 reads −.8VDC, then the meter should display ØdB minus 5dB, or −5dB (10dB scale), because −.8V is .5V below the full scale reading of −.3V. If the relationship between TP4 and the meter reading is correct, but the reading is not what is expected, then troubleshoot A22 (Service Group C).

8-B-73. If the signal at TP4 is correct but the meter reading is not, troubleshoot U19 and U20 according to the information given in Figure 8-B-8. Note the mathematical derivation of the voltage at U20 pin 7. If this is not correct then neither the meter reading nor the METER output will be correct.

8-B-74. If the voltage drop across the meter exceeds about 25 millivolts, it is probably open. Both terminals should be at approximately +1VDC with respect to ground at all times.

CAUTION

Do not attempt to measure the internal resistance of the meter movement with an ohmmeter, as destruction will almost certainly result.

8-B-75. Intermodulation Distortion.

8-B-76. Prior to troubleshooting IMD problems in this section, be sure to read and understand the discussions on distortion problems in paragraphs 8-A-36 through 8-A-44 and in Table 8-9. There is no point troubleshooting A10 and beyond if the signal arriving at A10 from A5 is at fault.

8-B-77. The only kinds of distortion that can originate in the IF section are intermodulation products of two or more signals that are within the IF bandpass of the instrument. Much information can be gained by observing the amount of distortion as a function of the IF bandwidth and the frequency separation of the input signals. Every point in the IF section has a bandwidth associated with it, as shown in Table 8-B-3. Two signals that are separated by greater than that amount cannot both pass that point, and can therefore not mix to cause intermodulation products past that point.

Table 8-B-3. IF Bandwidths.

Location	Bandwidth	Center Frequency	Selected Filter
Prior to A5T20	0-32.5MHz	Not Applicable	–
A5T20 to A10T3	± 5kHz	50.000MHz	–
A10T3 to A20TP8	± 5kHz	15.625kHz	(3100/2000/1740Hz Filter)
A10T3 to A20TP8	± 200Hz	16.625kHz	(400Hz Filter)
A10T3 to A20TP8	± 10Hz	15.625kHz	(20Hz Filter)
A20TP8 to A21TP1	± 1550Hz	15.625kHz	(3100Hz Filter)
A20TP8 to A21TP1	± 1000Hz	15.625kHz	(2000Hz Filter)
A20TP8 to A21TP1	± 870Hz	15.625kHz	(1740Hz Filter)

8-B-78. For example, assume that two signals, one at some tuned frequency f, and the other at f + 4kHz are observed to be causing IMD products at f ± 4kHz, f ± 8kHz, etc. When the signals reach the IF filter board (A20), frequency f has been converted to 15.625kHz and f + 4kHz to 19.625kHz. Because even the widest filter on A20 only passes 15.625kHz ± 1.55kHz the higher frequency component will not get through. For IMD to occur, however, two signals must be present. It can therefore be positively stated that nothing past the 3100/2000/1740Hz filter is causing the problem in this case.

8-B-79. Suppose, however, that the IMD is caused by input signals at f and f + 100Hz. Using the 3100/2000/1740Hz or 400Hz filters, both of the signals would be present all the way down through A21TP1, the input to the detector circuit, and intermodulation could be occurring anywhere. If the problem were to disappear, however, when the 20Hz filter was selected, the only portion of the IF path which no longer would be "seeing" both signals is the section past the 20Hz filter, which would therefore become the suspect area.

8-B-80. Using this type of logic, the source of IMD can be narrowed to a small number of stages. Those stages should then be checked for proper biasing, signal levels, alignment, etc. Some specific areas to watch are as follows.

8-B-81. The 50MHz crystal filters can be a cause of IMD. On the A10 board, this possibility can be eliminated by using the built-in bypass provision (see paragraph 8-B-17).

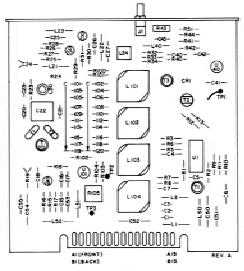
8-B-82. Insufficient or unbalanced 2nd L.O. drive is another possible cause of IMD. Check signal levels on A10.

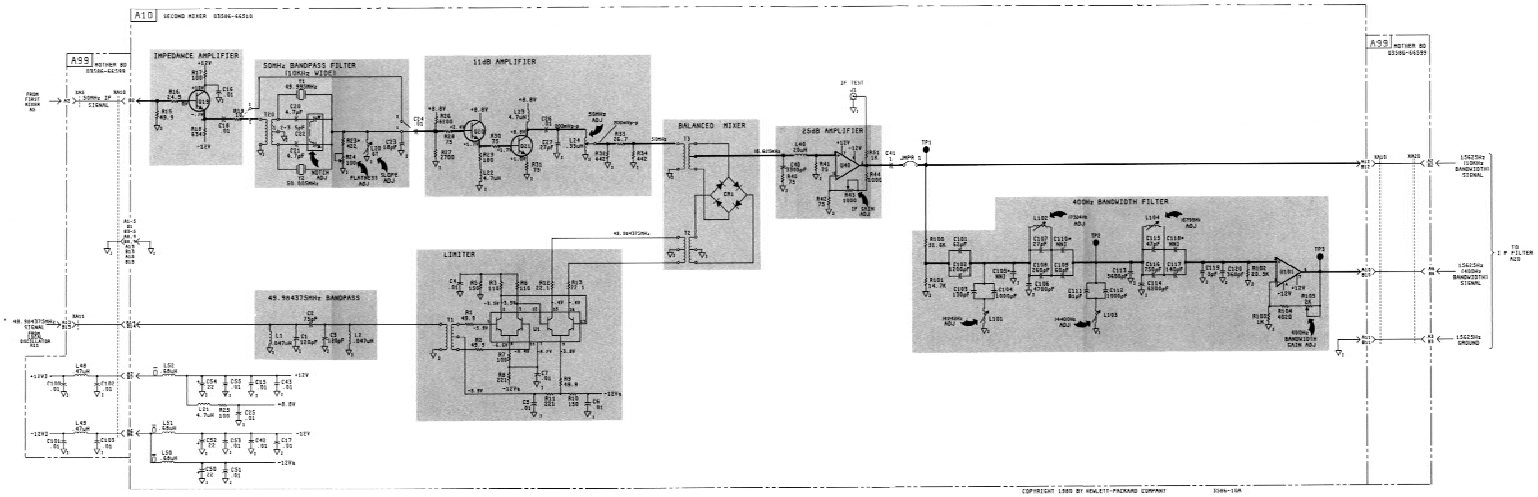
8-B-83. Spurious Signals.

8-B-84. Because the IF stages are all fixed tuned to either 50MHz or 15.625kHz, their capability for generating spurs is very small. Any spur that does occur will not be tuneable, that is, it will appear regardless of the frequency to which the instrument is tuned. Service Group D covers the isolation of spurs that occur at discrete input frequencies.

8-B-85. The IF stages are, of course, susceptible to picking up stray RF that may appear at the appropriate frequencies. Isolating the stage that is picking up the signal is as simple as pulling out PC boards (starting at the front end) until the spur disappears. Having isolated this stage, look for faulty shielding, poor grounds, etc.

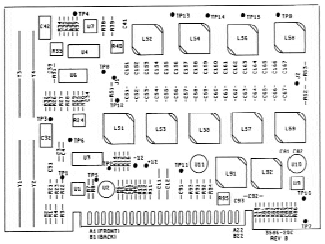
8-B-86. Self-oscillation of an IF stage will also cause a spurious signal to appear independent of tuning. Isolate to a specific stage using an oscilloscope, and check for faulty bypass capacitors, biasing resistors or other components.



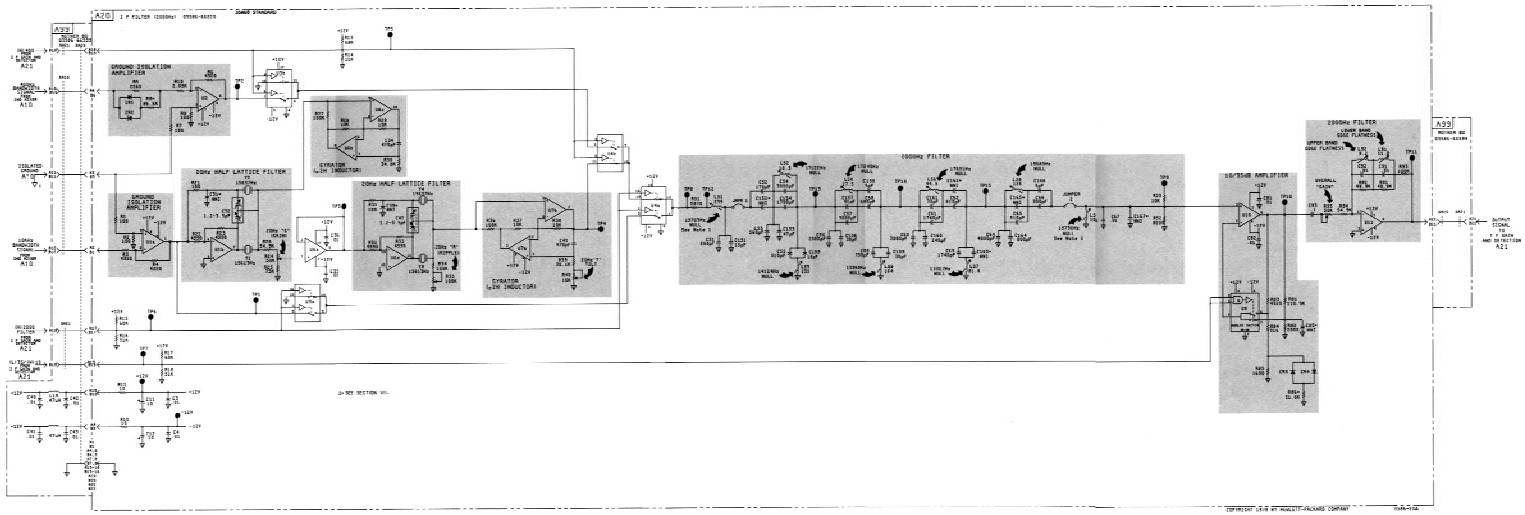


4

Figure 8-B-1. Schematic - Second Mixer (A10)

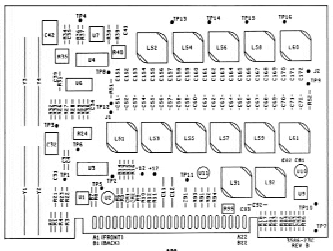


NOTES:
1. NULL occurs only when jumper 1 is removed.
2. NULL occurs only when jumper 2 is removed.
3. Some revision "A" P.C. boards are electrically identical to revision "B" boards.



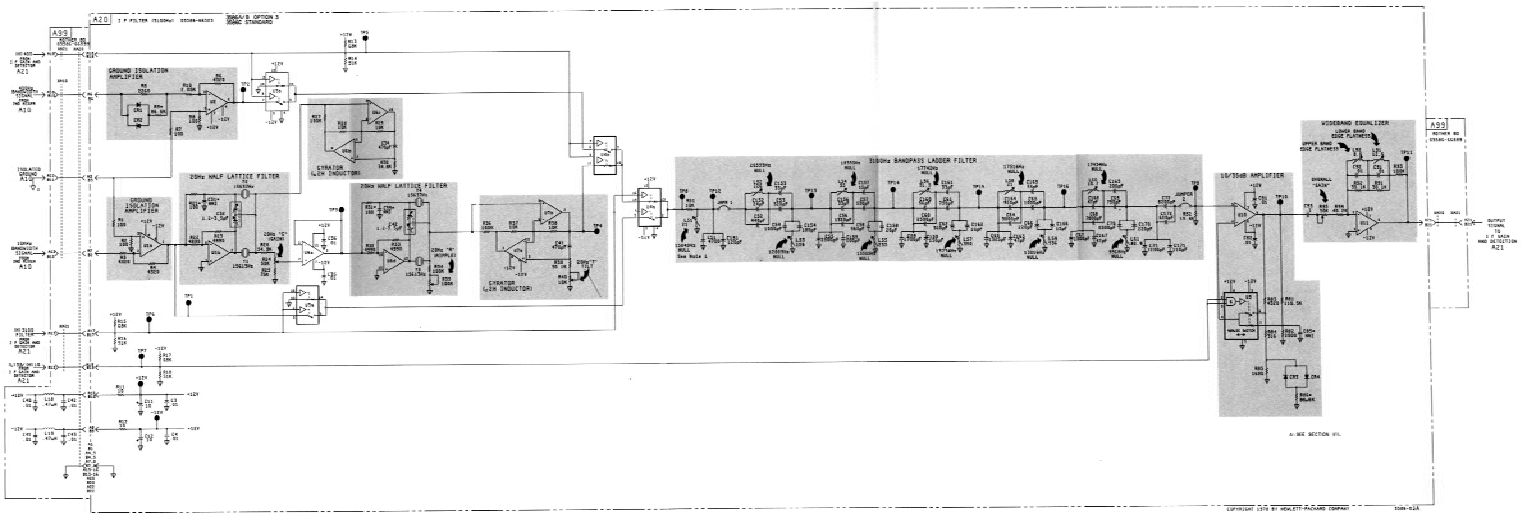
5A

Figure 8-B-2. Schematic - IF Filter (A20) - 2000Hz
8-B-13/8-B-14



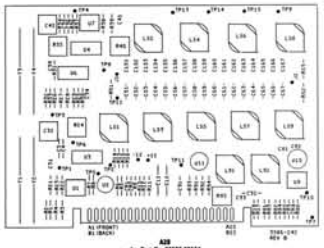
A20:
-hp Part No. 03588-60523
Rev B

NOTES:
1. NULL occurs only when jumper 1 is removed.
2. Some revision "A" P.C. boards are electrically identical to revision "B" boards.

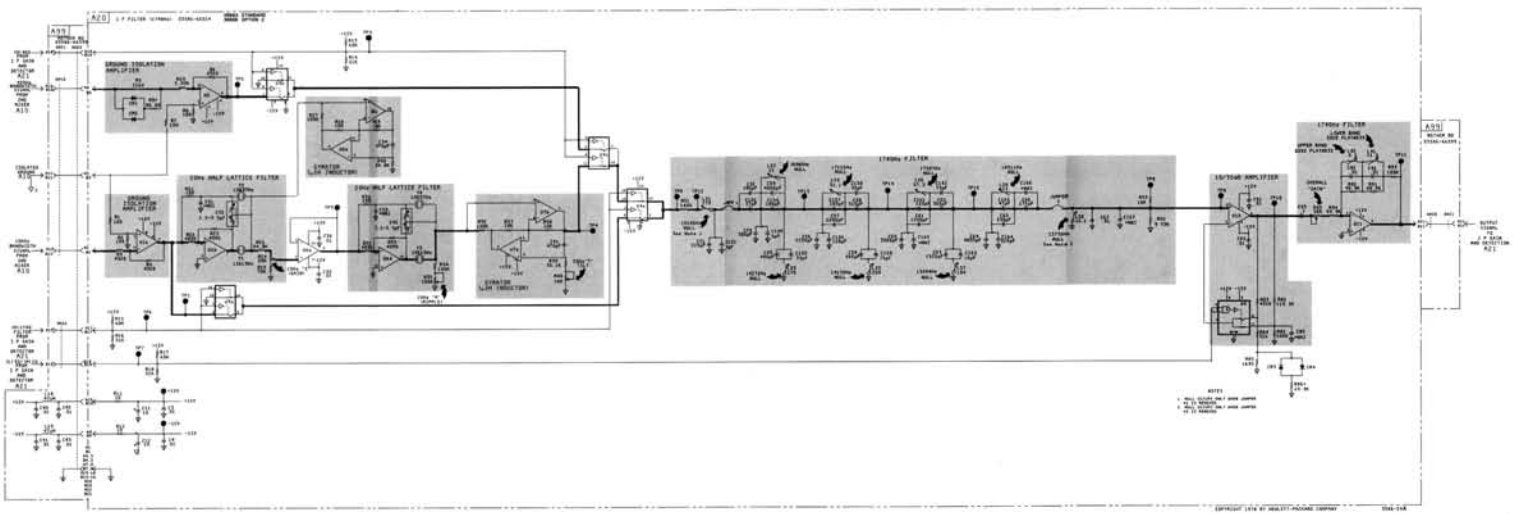


5B

Figure 8-B-3. Schematic - IF Filter (A20) - 3100Hz

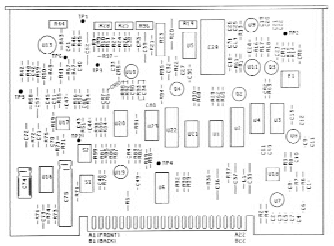


NOTES:
1. NULL occurs only when jumper 1 is removed.
2. NULL occurs only when jumper 2 is removed.
3. Some revision "A" P.C. boards are electrically identical to revision "B" boards



5C

Figure 8-B-4. Schematic - IF Filter (A20) - 1740Hz



A21
Hp Part No. 03586-66521
Rev B

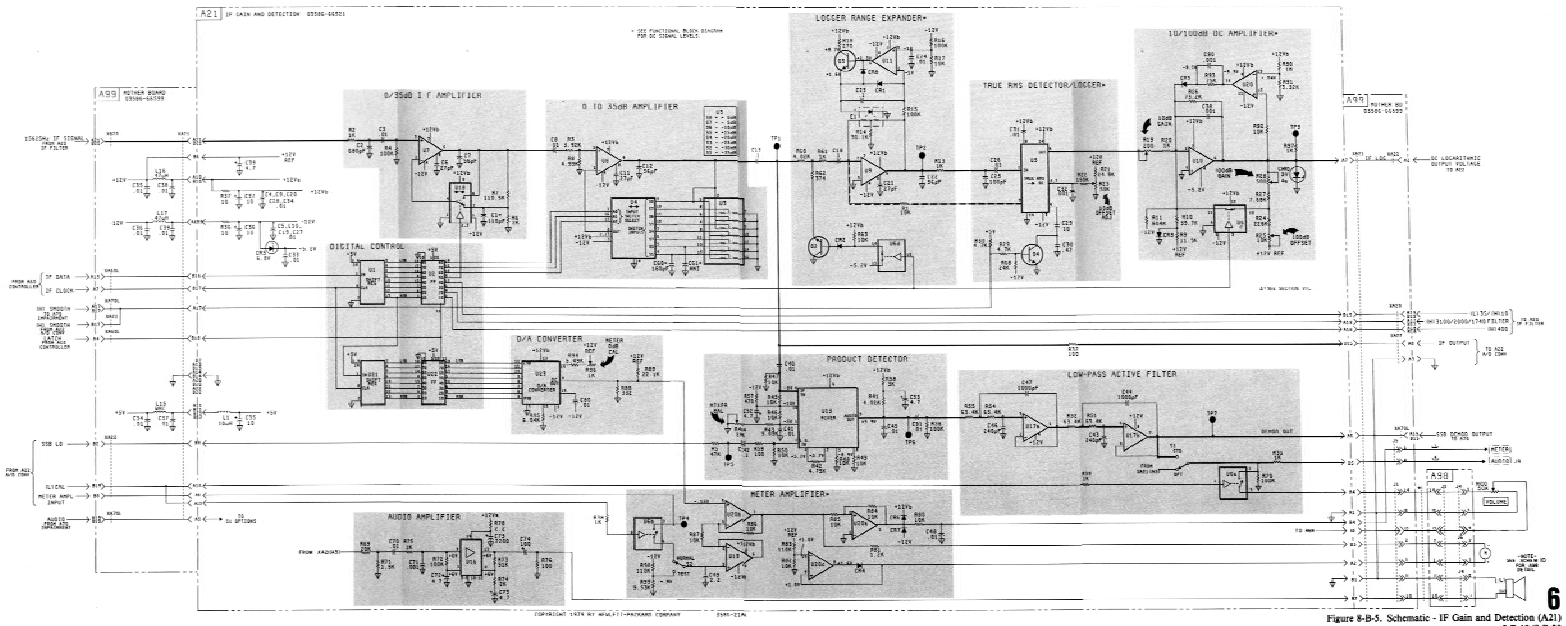
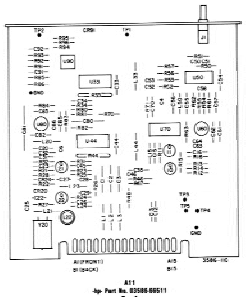


Figure 8-B-5. Schematic - IF Gain and Detection (A21)



A11
4p Part No. 83586-66511
Rev A

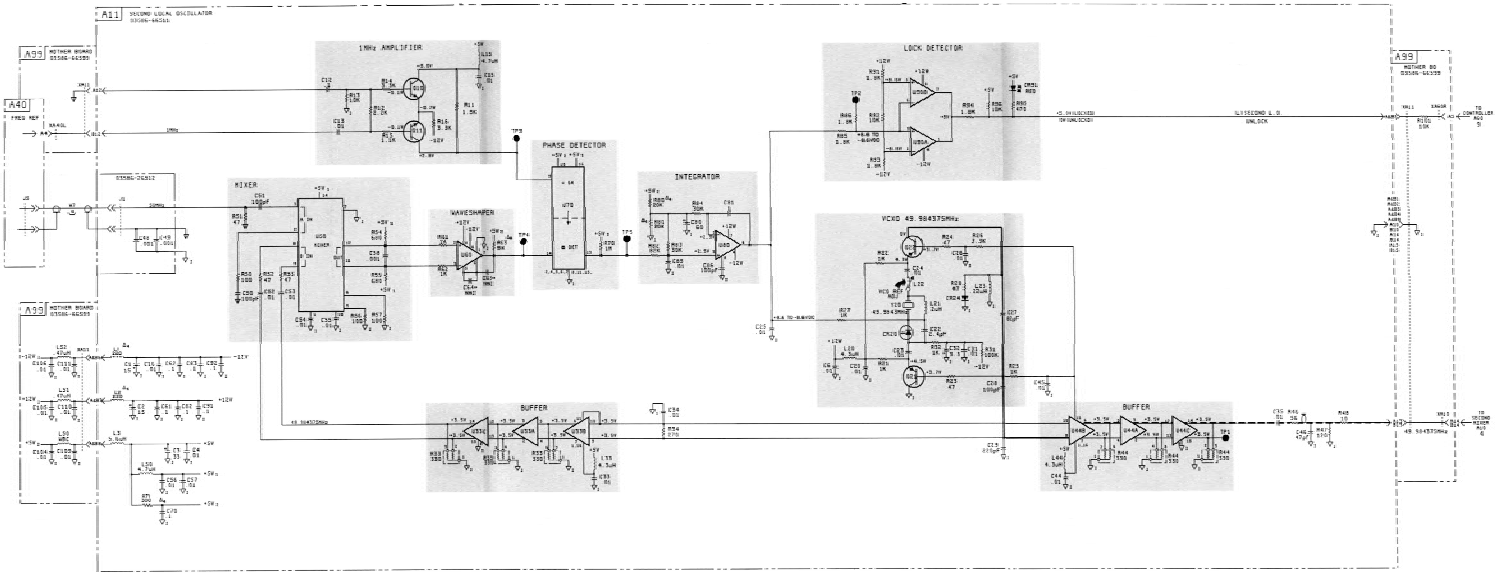
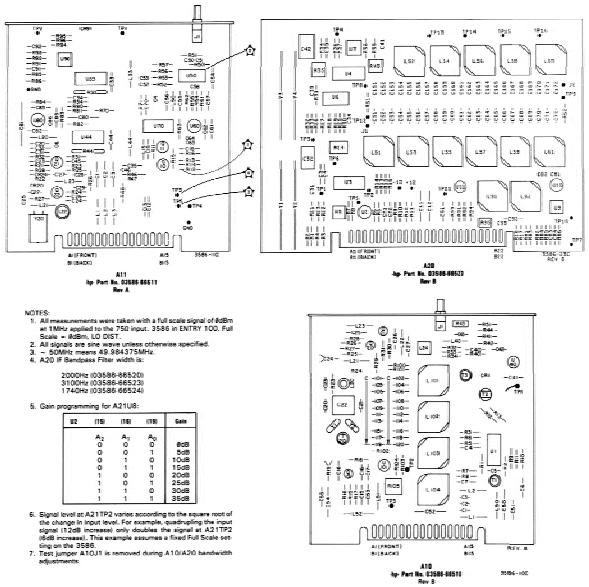


Figure 8-B-6. Schematic - Second Local Oscillator (A11)



NOTES:

1. All measurements were taken with a full scale signal of 6dBm at 1MHz applied to the 75Ω input, 3586 in ENTRY 10Ω. Full Scale = 6dBm, LO DIST.
2. All signals are sine waves unless otherwise specified.
3. ~ 50MHz means 49.38437SMHz.
4. A20 IF Bandpass Filter width is:

   200Hz (03586-66520)
   3100Hz (03586-66523)
   174Hz (03586-66524)

5. Gain programming for A21U8:

B2	(TS)	(TS)	(TS)	Gain
	A_2	A_1	A_0	
	0	0	0	0dB
	0	0	1	5dB
	0	1	0	10dB
	0	1	1	15dB
	1	0	0	20dB
	1	0	1	25dB
	1	1	0	30dB
	1	1	1	35dB

6. Signal level at A21TP2 varies according to the square root of the change in input level. For example, quadrupling the input signal (12dB increase) only doubles the signal at A21TP2 (6dB increase). This example assumes a fixed Full Scale setting on the 3586.
7. Test jumper A10J1 is removed during A10/A20 bandwidth adjustments.

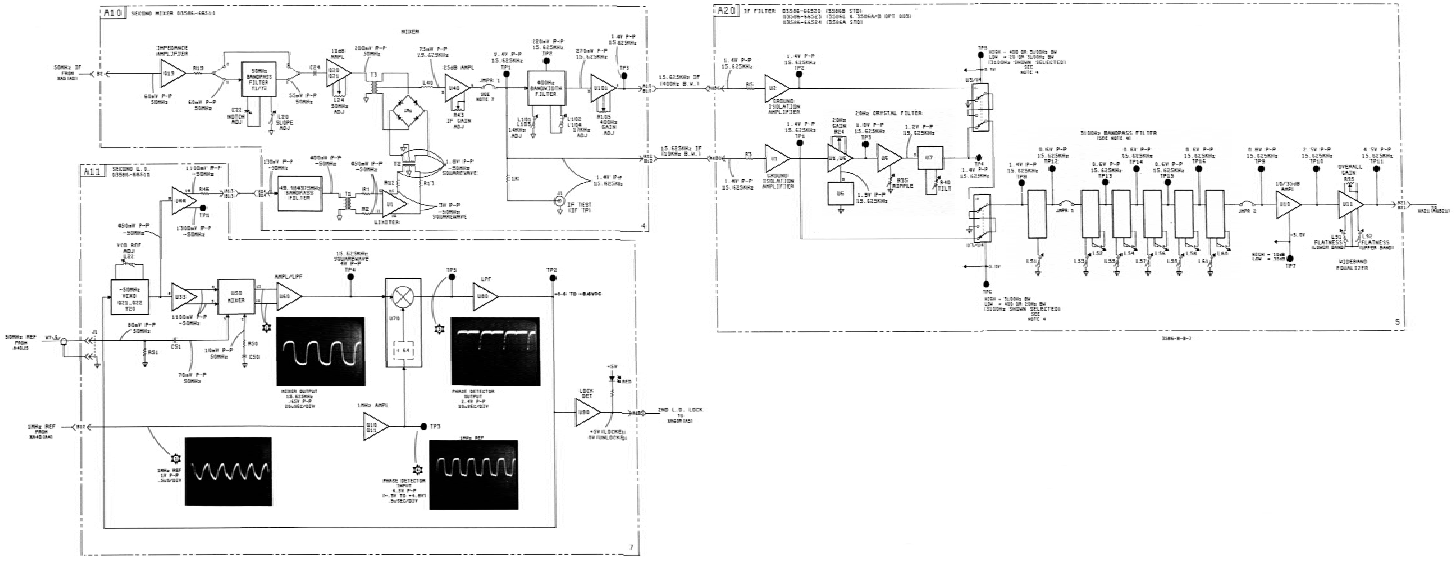
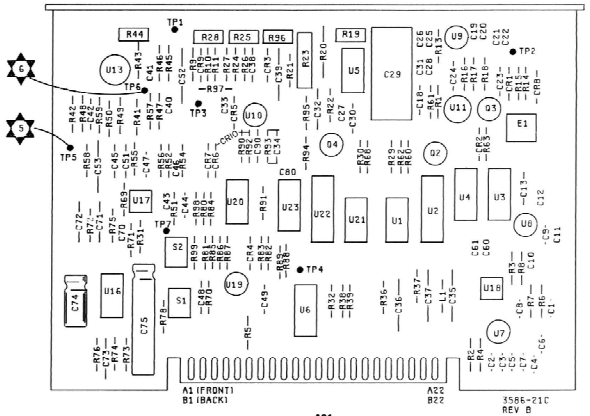


Figure 8-B-7. Functional Block (1 of 2) - IF/Audio (A10/A11/A20/A21)



A21
-hp- Part No. 03586-66521
Rev B

NOTES:

1. All measurements were taken with a full scale signal of ØdBm at 1MHz applied to the 75Ω input. 3586 in ENTRY 100, Full Scale = ØdBm, LO DIST.
2. All signals are sine wave unless otherwise specified.
3. ~ 50MHz means 49.984375MHz.
4. A20 IF Bandpass Filter width is:

   2000Hz (03586-66520)
   3100Hz (03586-66523)
   1740Hz (03586-66524)

5. Gain programming for A21U8:

U2	(15)	(16)	(19)	Gain
	A_2	A_1	A_0	
	0	0	0	ØdB
	0	0	1	5dB
	0	1	0	10dB
	0	1	1	15dB
	1	0	0	20dB
	1	0	1	25dB
	1	1	0	30dB
	1	1	1	35dB

6. Signal level at A21TP2 varies according to the square root of the change in input level. For example, quadrupling the input signal (12dB increase) only doubles the signal at A21TP2 (6dB increase). This example assumes a fixed Full Scale setting on the 3586.
7. Test jumper A10J1 is removed during A10/A20 bandwidth adjustments.

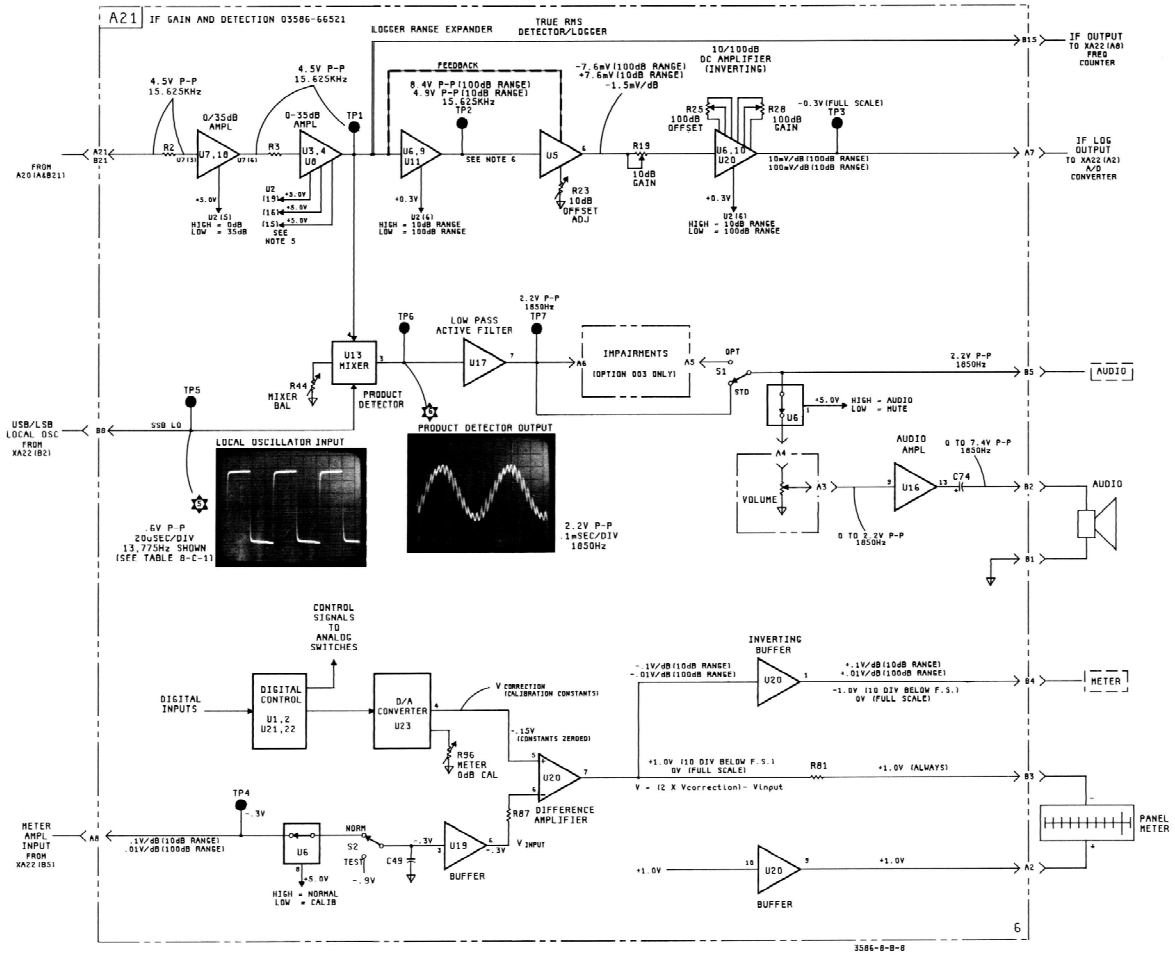


Figure 8-B-8. Functional Block (2 of 2) - IF/Audio (A10/A11/A20/A21)
8-B-25/8-B-26

Table of Contents

A/D CONVERSION, DIGITAL CONTROL AND DISPLAY SERVICE GROUP C

Contents

8-C-1. ADJUSTMENTS (CROSS REFERENCE).

8-C-2. A/D Converter Adjustments (A22).

Designation	Adjustment Title	Paragraph
A22R6	VCO Frequency Adjust	5-8
A22R21	Voltage Reference Adjust	5-8

8-C-3. THEORY OF OPERATION (CROSS REFERENCE).

8-C-4. A/D Converter (A22) - Paragraph 8-168.

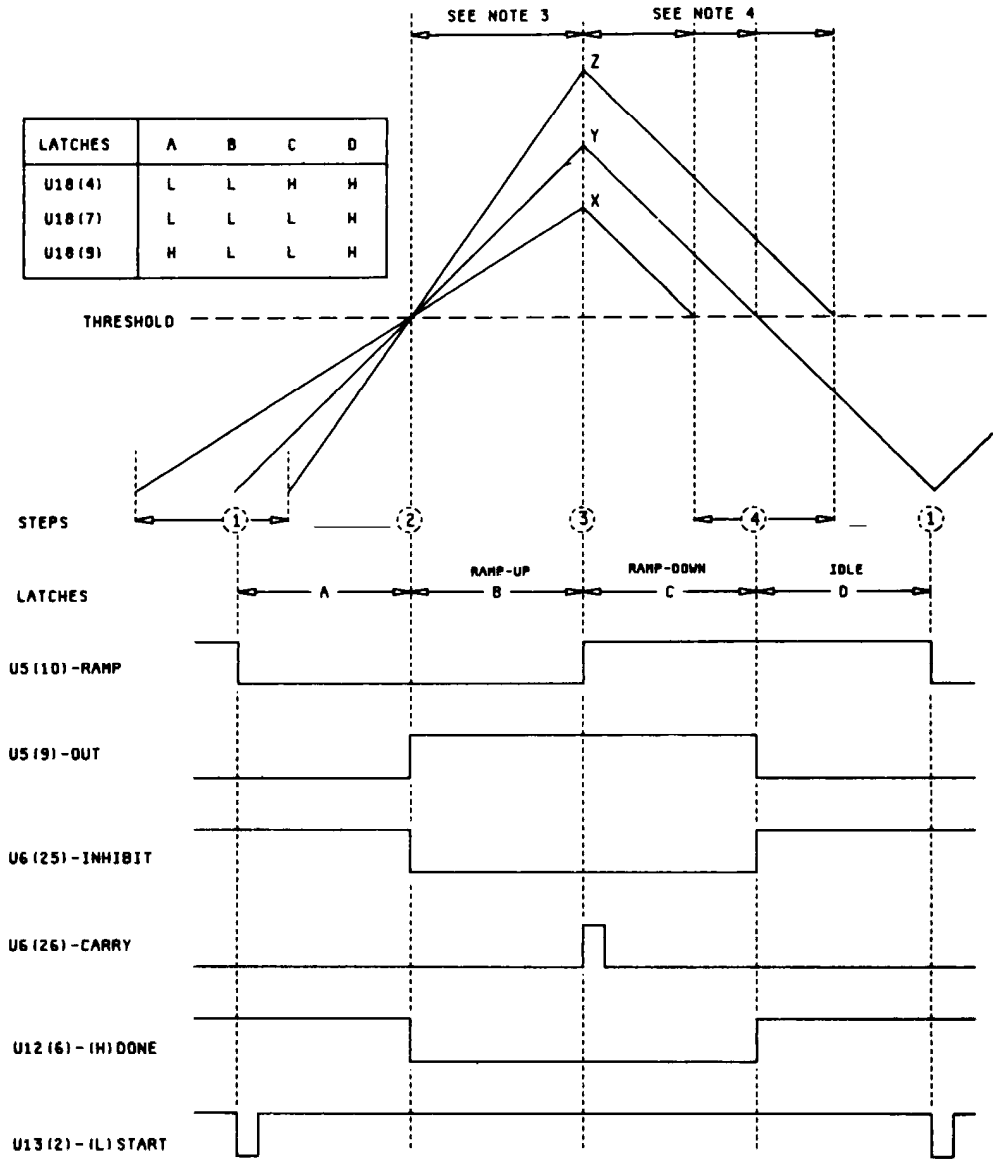
8-C-5. Controller (A60) - Paragraph 8-249.

8-C-6. Displays/Keyboard (A98) - Paragraph 8-265.

8-C-7. TROUBLESHOOTING DATA.

8-C-8. A/D Converter (A22) Troubleshooting.

8-C-9. Error Code Err 7. When error code Err 7 is continuously displayed, it indicates that the A/D Converter did not set the (H) DONE line to HIGH within two seconds after the A60 processor set (L) START to LOW. This would indicate that the Logic State Machine (LSM) on A22 is probably hung up in a static condition either because of a component failure within the LSM or because it did not receive an expected input. The LSM is asynchronous, i.e. it is not clocked but changes state when certain input conditions are changed (see Figure 8-C-1). If the LSM is stopped, awaiting one of its normal inputs, the latches in U18 should indicate what state (A-D) the LSM is in and thus what input it did not receive. This should help in isolating a failed component. An occasional, transient, Err 7 at turn-on or during auto-ranging which immediately goes away and does not return may be considered normal operation.



NOTES:

1. The ramp-up slope depends on the input voltage to U5 (pins 1 and 2). Z represents a high input and X represents a low input.
2. The ramp height represents the voltage across charging capacitor A22C7.
3. The time between steps (2) and (3) is a fixed time period, determined by the counter going from 990,000 to 1,000,000.
4. The time between steps (3) and (4) varies as a function of how large the input voltage was to U5 and therefore how high the charge on A22C7 became.
5. The ramp-down slope is a constant value for all inputs (set by A22R21).
6. Steps:

   (1) Processor pulses (L) START from HIGH to LOW, forcing "RAMP" from HIGH to LOW. Ramp starts up as A22C7 charges.

   (2) Ramp crosses threshold. U5 sets "OUT" from LOW to HIGH. Counter starts counting from 990,000. "(H) DONE" goes LOW.

   (3) Counter overflows at 1,000,000 from 500kHz pulses and begins counting upwards from zero. U6 pulses "CARRY" from LOW to HIGH, forcing "RAMP" back to HIGH. Ramp starts down as A22C7 discharges at a constant rate.

   (4) Ramp again crosses threshold after time period determined by height of ramp. U5 now sets "OUT" back to LOW. Counter stops. LSM sets "(H) DONE" back to HIGH. Processor now scans U6 for digital number representing value of analog voltage, presetting counter, LSM is idle.

Figure 8-C-1. A/D Conversion (Dual Ramp).

8-C-10. A/D Self-Test. TF8 (paragraph 8-73) is a quick self-test for the A/D Converter. When TF8 is activated, the processor commands A22U7 to select the input from pin 12 which is a voltage divider with about −1.1V present. This voltage is then converted by the A/D (when AUTO 10 is selected) to read between −125.5 and −130.3 in the MEASUREMENT DISPLAY area on the front panel. If the reading is correct with TF8 active, you know that U5, U6 and the LSM are all working correctly, i.e., the A/D conversion process is functional. Also, by multiplying the displayed reading by .0938, a reasonably accurate value for the −12V power supply voltage is obtained without removing any instrument covers. Since the +12V supply is the reference voltage for the −12V supply, by implication it must be good also. Nothing is known, however, about the +5V supply from this test.

8-C-11. Group test 3.2 under TF13 (paragraph 8-81) is a test for the Frequency Counter mode of the A22 board. If it fails, troubleshoot the Counter circuits as described in paragraph 8-C-17. See also paragraph 8-C-13.

8-C-12. A/D Troubleshooting Hints.

8-C-13. A quick way to divide the A22 board for troubleshooting is to use the Frequency COUNTER mode. Input a known frequency signal to the 3586 with an amplitude equal to the Full Scale setting with ENTRY 100 selected. For example, with a Full Scale setting of ØdBm, tune the 3586 to a frequency of 1MHz and then input a signal of 1MHz at ØdBm in LO DIST mode. If the amplitude display is not reading about ØdBm, press COUNTER. With 3100Hz bandwidth selected, vary the frequency of the input signal by several hundred hertz either side of 1MHz. The 3586 frequency readout should follow the input frequency change.

NOTE

Remember that the 3586 and the signal source must be phase-locked together for them to track exactly *in frequency.*

8-C-14. If the frequency readout tracks the signal source frequency in the COUNTER mode, then U4, U19, U20, U6 and all associated gates are working correctly. In addition, you know that the analog signal path from the input all the way up to, but not including, the A21 Detector/Logger circuit is functional. Therefore, any problem with the amplitude display of the input signal must be between the input to the A21 Detector/Logger and the A22 LSM, in the A/D Conversion path. Use TF8 (see paragraph 8-C-10) to test the A/D Converter itself. If good, either the Input Data Selector (U7) is not switching correctly or the problem is on A21 (see Service Group B for troubleshooting of the A21 Detector/Logger circuits). If TF8 fails, the problem is most likely on A22. Check the Data Selector (U7) in paragraph 8-C-15.

8-C-15. To verify U7 operation *and* to verify the A21 Detector Logger output, again input a full scale signal as described in paragraph 8-C-13. Connect a DVM across A22TP1 and A22TP2. The DVM should read a full scale (equivalent) voltage of −.3VDC with LO DIST and with WIDEBAND selected. If TF8 is now activated, the DVM should read −1.1V. Again selecting WIDEBAND or LO DIST should cause the DVM to read −.3V as the selected input is passed through U7 to TP1. All of the logger inputs to A22 are linear, referenced to the Full Scale setting. At Full Scale, the input should be −.3V. At 10dB below Full Scale, the voltage should be −.4V. At 20dB below Full Scale, it should be −.5V and so forth, down to the end of the linear operating range of the logger chips at about 80dB below Full Scale, where the DVM should read −1.1V. If the DVM reads correctly, U7 is working and the input signal from the Logger is correct.

8-C-16. Because of the complexity of the A/D Conversion process there is no simple way to troubleshoot the LSM if the U18 Latches are not in a static condition (see paragraph 8-C-9). The service technician must simply check the various inputs and outputs which should be toggling until a bad component is found. The following checks should help.

1. Look at U5(7) with a scope. If U5 is cycling correctly, the dual slope ramp should be clearly visible at a 3-4Hz rate (about 1.5Vp-p Full Scale) with the COUNTER off, and at a 2Hz rate with the COUNTER on. If not, check to see if the RAMP command signal at U5(10) is present. If yes, and a full scale signal (−.3V) is present at U5(2), then U5 is probably bad. If the dual slope ramp is present, one of the LSM gates or latches may be bad.

2. If the frequency COUNTER is not working *and* the amplitude readout is not working, suspect U6, U8 and U11. With the COUNTER off, look for 500kHz at U6(24). If present, check for an input of 6 pulses grouped together at the SCAN line every half-second. If present and U6(5-8) are not toggling, U6 is probably bad. If the 500kHz is missing, signal trace backwards through U8(3), U11(4), and U11(1) to U16(12) where it originates. If missing at U16(12), check the 1MHz input to the ÷ 10 circuits. The line into U16(14) and the other decade counters (U14 and U15) is a CLEAR signal which should be cycling at 2Hz only when the COUNTER is on. The 1Hz clock at U14(13) is only visible when the COUNTER is off.

3. With the COUNTER off, U2(19) should be always LOW. With the COUNTER on, U2(19) should be HIGH with narrow pulses to LOW and back to HIGH every half-second. This is the command signal which switches the LSM between the A/D mode (U2(19)LOW) and the COUNTER mode (U2(19)HIGH).

4. The A/D process is started by the processor pulsing (L) START to LOW from its normally HIGH state. This is a single, very narrow pulse, occurring every half-second, so look for it carefully before assuming it is missing. However, if Err 7 is displayed because (H) DONE is stuck LOW, this pulse *will* be missing and the A/D process cannot begin without the START pulse. One way to check the processor operation in this regard is to momentarily ground XA22(B20). If the Err 7 code was not displayed previously, it should be with the (H) DONE line shorted to ground (after 2 seconds).

5. With the normal range of input voltage to U5 (−.3V to −1.1V), the A/D "idle" time (between ramps) should be about ten (10) times the width of the dual slope ramp time with the COUNTER on. With the COUNTER off, the idle time should be about 3 to 4 times the ramp time. If these conditions are not true, U5 may be bad or R21 may need adjusting (paragraph 5-8).

6. Normal operation of the U18 latch outputs is all three (pins 4, 7, and 9) HIGH with the COUNTER off, but pulsing LOW very briefly at a 3-4Hz rate. When the COUNTER is on, pins 4 and 7 remain HIGH in the idle state, pulsing LOW briefly every half-second, but U18(9) is now normally LOW in the idle state, pulsing HIGH briefly every half-second.

8-C-17. Counter Inoperative. If the COUNTER does not appear to be working, or it definitely fails the Group 3.2 subtest of TF13 (paragraph 8-81), proceed as follows.

1. Check XA22(A8) for a 15.625kHz sine wave at about 4Vp-p for a Full Scale signal input. If missing, proceed to Service Group B and troubleshoot the second I.F. signal output to A22. If present, check U4(3) for a 15.625kHz (f_O) square wave at 12Vp-p referenced to 0 volts DC. Check U20(14) for 12Vp-p from +12V to ØV. Check U20(4) for 312.5kHz ($20f_O$) at 12Vp-p (+12V to ØV).

2. If the $20f_0$ signal is missing at U20(4), lift either end of R11. The voltage at the junction of R12 and R13 (about +7.2V) should drive the VCO to about 350kHz. If it does, U4 is probably bad although U19 should be checked to see if U19(3) has 15.625kHz present with 312.5kHz at U19(9). If the VCO is not running with R11 lifted, U20 is probably bad.

3. If U20(4) has 312.5kHz present, check U6(24) to see that it is alternating between 312.5kHz and 500kHz every half-second with COUNTER on. If not, one of the gates in U11 or one of the buffers (U8 or U17) is probably bad or U2(19) is not switching with the COUNTER on.

8-C-18. LSB/USB Oscillators.

8-C-19. The signal present at TP101 may be any one of eight (8) different frequencies (see Table 8-C-1) depending on the 3586 model number (A/B/C), whether option 003 (A70 Impairments) is installed, which sideband (LSB or USB) is selected, and whether CAL is active. If no signal at all is present, troubleshooting should be fairly straightforward.

Table 8-C-1. Single Sideband (SSB) LO Frequencies.

Model	Opt. 003	CAL Active	Bandwidth	Sideband	Crystal	Crystal Freq.	SSB LO Freq.	A22 Part Number
3586A/B	YES	NO	3100Hz	USB	A22Y102	1.7475MHz	17.475kHz	03586-66522
3586A/B	YES	NO	3100Hz	LSB	A22Y101	1.3775MHz	13.775kHz	03586-66522
3586A	YES	YES	3100Hz	**	A70Y1*	1.6425MHz	16.425kHz	03586-66522
3586B	YES	YES	3100Hz	**	A70Y1*	1.6625MHz	16.625kHz	03586-66522
3586A#	NO	NO	1740Hz	USB	A22Y102	1.6975MHz	16.975kHz	03586-66526
3586A#	NO	NO	1740Hz	LSB	A22Y101	1.4275MHz	14.275kHz	03586-66526
3586B	NO	NO	2000Hz	USB	A22Y102	1.7125MHz	17.125kHz	03586-66525
3586B	NO	NO	2000Hz	LSB	A22Y101	1.4125MHz	14.125kHz	03586-66525
3586C	##	NO	3100Hz	USB	A22Y102	1.7475MHz	17.475kHz	03586-66522
3586C	##	NO	3100Hz	LSB	A22Y101	1.3775MHz	13.775kHz	03586-66522

NOTES:
* 3586A - A70 Part No. 03586-66571
3586B - A70 Part No. 03586-66570
** Don't Care.
\# The 3586B (without Opt. 003) has 1740Hz bandwidth available as Opt. 002. It also uses 03586-66526.
The 3586C is not available with Option 003.

8-C-20. First, try to select other frequencies according to Table 8-C-1. If you can, U101B is switching correctly and the source circuit for the bad signal is probably defective. If no signals at all can be seen at TP101, check to see if pins 3, 4, or 5 are stuck LOW and if so, chase down the short. Normally, two of these pins are solid HIGH while the selected signal on the third pin is oscillating at the signal frequency.

8-C-21. Note also that U2(6) selects USB when HIGH by enabling U101(10) and by turning on Q101 and shorting U101(1) to ground to shut off LSB. U2(6) selects LSB when LOW by disabling U101(10) and enabling U101(1) with Q101 shut off. Also, U2(9) shuts both LSB and USB off when LOW by disabling U101(2 and 11) whenever CAL is active. The LOW at U2(9) also goes to A21 during CAL to disconnect the panel meter and mute the speaker. Also, during CAL, the processor sends a command to A70 (if installed) to activate the CAL OSCillator signal which comes to A22 through XA22(B3) and is the third switchable input to U101B.

8-C-22. Check also that the ÷100 circuit is working correctly when there *is* a signal at TP101.

8-C-23. Controller (A60) Troubleshooting.

8-C-24. Since the microprocessor on the A60 Controller board governs all 3586 operations, it must be working correctly in order to check almost all other functions/capabilities of the 3586. If the operator can select measurement modes, enter frequencies, and select and run internal self-tests (see paragraph 8-49) satisfactorily from the front panel in the Local mode, basic processor operation can be assumed as being normal. Any remaining Controller board problem is usually associated with an input/output operation and, by logical reasoning, can usually be isolated to a particular IC chip as the most likely candidate for failure.

8-C-25. If basic processor operation is defective, it is usually manifested by such symptoms as flickering or frozen displays, nonresponsive keyboard switches or unstable readings. Errors in readings or measurements are usually due to a single defective IC chip or, sometimes, to open or shorted data lines. Frozen displays or non-responsive switches often indicate loss of a clock pulse or a single stuck switch.

8-C-26. If the 3586 does not initialize correctly at turn-on, often *what it does do* is a possible indicator of where the problem lies. Paragraph 8-C-34 discusses all of the various problem symptoms that might lead the operator or service technician to suspect the A60 Controller board as having a problem. Directions on how to proceed are also given for each symptom.

CAUTION

The A60 Controller board contains CMOS devices (U28 and U29) which are extremely susceptible to static electricity damage. It is especially important that grounded tools and wriststraps be used when handling or repairing the A60 board. All standard service procedures for preventing static electricity component damage should be followed for storing, transport, and handling of A60U28 and A60U29.

8-C-27. ROM Software Differences. The ROM's on the A60 board have one of two different software configurations, Revision A or Revision B. ROM's A60U7-U12 therefore have different part numbers for the two software revisions as shown in Table 6-3 (see Section VI). Revision A ROM's should be available as replacement parts during the warranty period of all instruments delivered with Revision A software. Individual ROM's are not interchangeable between revisions. A complete *set* of Revision B ROM's is a direct replacement for a complete set of Revision A ROM's but a capacitor change on the A4 board is also required at the same time. ROM identification is possible in three ways.

1. Part Number (see Table 6-3).

2. Turn-on input impedance selection:

   75 ohm termination - Revision A
   10K ohm termination - Revision B

3. TF14 (see paragraph 8-82). - Displayed date of 7-23-79 is Revision A. Displayed date of 6-30-80 is Revision B.

8-C-28. The Revision B software provides increased program stability, corrects some non-specification-related algorithm errors, adds a factory-settable "special instrument" configuration index, and provides a Slow Autorange capability not available in Revision A ROM's.

8-C-29. Fast/Slow Autoranging. In the Revision B software, a fast/slow autoranging routine is implemented for front-end (RF section) autoranging. Whenever the input spectra to the 3586 is varying in power level by several dB at a frequency rate of less than 50Hz, poor autoranging performance is a possible result. Selecting AVEraging can help alleviate this problem, but with the tradeoff of a slower measurement sampling rate. The slow autoranging mode can help to overcome the problem of continuous autoranging by reducing the susceptibility of the broadband power detection circuits to fluctuating input power levels. A different component value for an A4 board capacitor plus a switch setting change on A60 are required to implement slow autoranging (see paragraph 8-C-32 and Table 8-C-3). If the instrument is selected for slow autoranging, TF13 will fail because of automatic selection of dB .775V in SLOW. Put A60S2(7) in FAST to run TF13 (see Table 8-C-3).

8-C-30. Controller Timing. The processor (U6) should run if the supply voltages are present and the clock generator (U5) is running to provide clock pulses for basic hardware timing. Display timing for both scanning the keyboard switches and time-sharing the LED's in the frequency and measurement displays is provided by U20. U20 is a one-shot that generates a .5 millisecond pulse after it is reset by the processor. This pulse is the basic software timing clock for the program. It normally occurs at about 1900Hz at U20(3) and is slightly unstable due to processor reset not always being exactly on time. Since the display scan circuits on A98 have 19 controllable items to be scanned, the Display Scan Rate is about 100Hz. (See TF11 in paragraph 8-78). If this clock is running too fast or too slow, some timing problems could occur which might be mistaken for a faulty processor. If TF11 shows the scan rate to be other than 90-110Hz, try replacing U20 before doing anything else for erratic processor operation.

8-C-31. Clock Generator U5 should be running at about 3.8MHz for hardware timing. This frequency does not have to be exact as long as it is not close to 4MHz where spurs would be generated within the instrument. A range of 3.0MHz to 3.9MHz can be considered normal. See paragraph 8-C-54 for a troubleshooting discussion of the clock circuits.

8-C-32. Controller Switch Selections. There are two DIP-switch packages on A60, S1 and S2. These switches are used for selecting input termination configurations, special tests, and option/model configurations. Before changing any of these switches, for any reason, record the present settings for future reference. The switch definitions are different for Revision A software than what they are for Revision B. Be sure of which software revision your instrument has (paragraph 8-C-27) before changing switch positions. Use Table 8-C-2 for Revision A ROM's and Table 8-C-3 for Revision B ROM's.

8-C-33. If A60S1 (1 or 5) are in the Closed position at turn-on, the processor will appear to be not running (displays frozen, keys not responsive). A60S2 Contacts in the wrong position (by themselves) will not cause processor problems but will result in instrument misidentification to the processor and therefore measurement errors will occur.

8-C-34. Controller Problem Symptoms.

8-C-35. Turn-on Problems. When the 3586 does not complete its turn-on initialization sequence correctly, the problem could be on A60 but could also be due to a power supply pro-

blem, loose cable connectors, boards not seated, etc. Before assuming the Controller is at fault, review the information outlined in paragraphs 8-27 through 8-31, or use the Turn-On Troubleshooting flowchart at the end of the "Turn-On" section to eliminate these other problem sources. If the A60 is then still suspect, proceed to paragraph 8-C-41.

Table 8-C-2. A60 Switch Settings (Rev. A Software) (Terminated).

A60S1 (Five-contact DIP-Switch)

Contact	Closed (Up)	Open (Down)
1	Resets Processor (followed by open)	Normal Operation
2	Not Used	Not Used
3	Not Used	Not Used
4	Interrupts Processor to Test Routine (followed by open)	Normal Operation
5	Processor Kernel Test	Normal Operation

A60S2 (Eight-contact DIP-Switch)

Contact	Closed (0)	Open (1)
1	3586A or 3586C	3586B
2	3586A (Standard) or 3586B (Standard)	3586A (Option 003) or 3586B (Option 003) or 3586C
3	3586A or 3586B	3586C
4	"Hz" (3586C)	"kHz" (3586A or 3586B)
5, 6, 7, 8	Used to select test modes (See Table 8-C-9)	

8-C-36. Front Panel Dark. Follow the procedures under "Front Panel Dark" in Table 8-9. If those procedures still point to the A60 board, proceed to paragraph 8-C-41.

8-C-37. Front Panel Flickering. Follow the procedures under "Front Panel Flickering" in Table 8-9. If those procedures still point to the A60 board, proceed to paragraph 8-C-41.

8-C-38. Front Panel Frozen. If the front panel displays are frozen in any configuration and/or the keyboard switches are not responding, cycle the POWER switch first. If the condition does not change, check that the blue 34 pin cable from A60 to A98 is fully seated at both ends and that the A60 board is fully seated. If these checks are good, verify that none of the contacts on A60S1 are in the up (closed) position (see Table 8-C-2). If the switch positions are correct, proceed to paragraph 8-C-41.

8-C-39. Store/Recall Inoperative. If the STORE/RECALL function switches are not working correctly, first remove the A60 board and verify that V-BAT is +2.2V to +2.8V at XA60L (A10) with the line power cord completely disconnected. If bad, proceed to Service Group J and troubleshoot the battery charging/regulating circuits. If the battery circuits are good, replace battery A80BT1. If V-BAT is good, plug in the line power cord, place the POWER switch in STANDBY and again check XA60L (A10) for +2.2V to +2.8V. If bad, proceed to Service Group J and troubleshoot the battery charging/regulating circuits. If

good, reinstall the A60 board and troubleshoot the V-BAT line components A60CR4, CR5, CR6, CR8, C34, C36, and Q1 using Figure 8-C-5. If those components check good, replace the CMOS RAM's (U28 and U29).

Table 8-C-3. A60 Switch Settings (Rev. B Software) (10kΩ).

A60S1

Same switch definitions for A60S1 as for the Rev. A software (see Table 8-C-2).

A60S2

Contacts 1	2	3	Measurement Group Switches
0	0	0	3586A (Standard)
0	1	0	3586A (Option 003)
1	0	0	3586B (Standard)
1	1	0	3586B (Option 003)
X	1	1	3586C

4	5	6 **	Termination Group Switches
0	0	0	3586A Standard
0	0	1	3586A with 150Ω/10kΩ in place of 600Ω
1	0	0	3586B Standard
1	0	1	3586B with 135Ω/10kΩ in place of 600Ω
0	1	0	3586C with 600Ω Bridged
0	1	1	3586C with 150Ω Bridged
1	1	0	3586C with 900Ω Bridged
1	1	1	3586C with 135Ω Bridged

7 **	Fast/Slow Autorange*
0	Fast (A4C40 = 1μF)
1	Slow(A4C40 = 10μF)

8 **	Hz/kHz Frequency Display
0	Hz (3586C)
1	kHz (3586A/B)

NOTES:
1. *Requires that A4C40 be changed to value indicated when switch position is changed.
2. ** Contacts 5-8 are also used to select test modes in conjunction with A60S1(4). See paragraph 8-C-46.
3. Contacts: 0 = Closed, 1 = Open, X = Don't Care.

CAUTION

Use grounded tools and wriststraps when handling CMOS RAM's. They are extremely susceptible to static electricity damage.

8-C-40. I/O Problems. If some keys work but others don't, or display readouts are missing segments or even whole numbers, it is possible that one of the input/output chips on A60 is bad. Other indications of a bad I/O chip are incorrect First L.O. Frequency or HP-IB problems. Troubleshooting this type of problem is best done through analysis to start. Milk the front panel for all the information you can get on the exact nature and details of the problem. Use the system block diagram and information-gathering procedures in Service Group K to determine what signals are missing or are in error. For a suspected bad key switch or a bad LED, run the Keyboard Test (paragraph 8-C-64) or the Display Test (paragraph 8-C-62) to see if any other failures are evident. For multiple switch or LED failures, it may be possible to identify a common line, clock signal or IC. Then examine the A60 schematics, using logical reasoning to identify possibly defective components. Finally, use standard digital troubleshooting procedures to check suspected components.

8-C-41. Controller Self-Tests.

8-C-42. Front Panel Digital Test (TF14). If the front panel is dark or frozen or flickering (and the power supplies are good), TF14 can not be run. Proceed directly to paragraph 8-C-44. If the A60 Controller and the A98 Switch/Display boards are working to the extent that the processor is at least responding to key depressions, try running the digital self-test (TF14) described in paragraph 8-82. It is implemented by pressing RECALL, • , CNTR→FREQ, 9 in sequence. If it passes this test, you know that the processor itself is good together with the clock generator circuits or the test could not have run to completion. You know that the ROM Select and RAM Select chips are working since the test program came from several ROM's and since it wrote a test pattern into the RAM's and then read it back from RAM memory to verify it. The test performs a checksum on ROM memory so the ROM's themselves must be good. You also know that at least some of the input multiplexing circuits are working to process keyboard switch depressions and the display output circuits are working because you could see the displayed test results plus the date of the ROM software revision in the right side display area. This also implies that the display refresh timer circuit (U20) is at least functional.

8-C-43. If FAIL is displayed when the digital self-test is run, a lit key LED will identify where the test failed. Use Table 8-C-4 to identify what failed. If a ROM failed, proceed to paragraph 8-C-45. If a RAM failed, proceed to paragraphs 8-C-46 and 8-C-47. If the results of the test are anything other than PASS or FAIL (e.g., blank displays) or if the test cannot even be accessed due to non-responsive keys or blank displays, proceed to paragraph 8-C-44 and test the processor. If the processor is good, continue with the other tests in paragraphs 8-C-45 through 8-C-49 until the bad component is located.

8-C-44. Processor Kernel Test. To establish that basic processor operation is correct, the processor must be isolated from the data bus and the rest of the digital devices, and then examined by itself. The kernel test accomplishes this.

1. Place the A60 board on two extender boards for easy access.

2. Carefully remove A60J1 (DIP shorting assembly) and A60U13 (ROM data buffer) from their sockets. This isolates the processor data bus lines from everything except the bus pull-up resistors and A60S1(5).

3. Place A60S1(5) in the up (closed) position and A60S1(1-4) in the down (open) position. This places a constant instruction (CLRB) on the data bus which the processor will execute over and over, incrementing the address bus by one number each time, and thus cycling through every possible address combination in sequence. As the data from each address is requested from ROM memory, the ROM's will try to place the data on the data bus. However, with U13 pulled, the processor is isolated from that data.

4. If a 5004A Digital Signature Analyzer is available, proceed to Step 7. If not, place a scope on U6 pins 9-20 and 22-25. Each of these lines should be "wiggling" at a constant frequency, with each line being twice the frequency of the line next to it, beginning at line A15 (pin 25) and descending down to line A0 (Pin 9).

5. Using the scope (DC coupled) or a DVM, check the data bus for +5V (HIGH) on pins 27 and 29-33 of U6. If any of these lines are ØV (LOW), there is a short on that line. Locate and clear the short before continuing. Pins 26 and 28 of U6 should have about +.6V on them due to diode drops across CR1 and CR2 with S1(5) closed. Open S1(5) and again check pins 26-33 of U6. They should now all be pulsing (TTL). Close S1(5) again.

6. Now check the following pins on U6 for about +5V: pins 2,4,5,6,8,34, and 40. Next check the following pins on U6 for ØV: 1,3,7,35,37,38, and 39. Next check pin 36 for about +2.8V. If any of these pins have the incorrect value present, look for any obvious damage to the PC board an then replace the processor (U6).

7. If a 5004A Signature Analyzer is available, connect the control leads as indicated.

Clock - U5(7) - Falling edge
Start - U2(9) - Rising edge
Stop - U2(12) - Falling edge

8. Check that the +5V signature is 0001 and the ground signature is 0000 before proceeding. If not, recheck your connections first and then use a scope to check for the clock signals at U2(9,12) and U5(7). If the signal at U5(7) is missing, check U5(3) for the 3.8MHz basic hardware clock. If missing, replace U4. If present, replace U5. If the signal at U2(9,12) is missing but the clocks at U6(3,36,37) are present, replace U6.

9. If the +5V and ground signatures are good, check the signatures on the pins of U6 and U24 according to Table 8-C-5. If any of the signatures are bad, check the +5V supply and the clocks (paragraph 8-C-54) first, then replace the IC. If replacing the IC doesn't correct the problem, check for opens or shorts on the affected lines. Check also for two lines shorted together.

10. If the processor (U6) signatures and the ROM Select (U24) signatures are good, the processor kernel test is complete and the processor (barring intermittent operation) is probably good. Proceed to paragraph 8-C-45.

Table 8-C-4. TF14 Failures.

Lit Key LED*	Failed Module
10dB	ROM A60U12
100dB	ROM A60U11
AUTO	ROM A60U10
ENTRY	ROM A60U9
AVE	ROM A60U8
dBm	ROM A60U7

* Any lit key LED other than those listed indicates a possible faulty RAM.

Table 8-C-5. Processor Kernel Test Signatures.

0000	1	40	0001	
0001	2	39	0000	
*0000	3	38	0000	
0001	4	37	0000*	
0001	5	36	0001*	
0001	6	35	0000	
0000	7	34	0001	
0001	8	33	0001	
5555	9	32	0001	
CCCC	10 U6	31	0001	
7F7F	11	30	0001	
5H21	12	29	0001	
OAFA	13	28	0000	
UPFH	14	27	0001	
52F8	15	26	0000	
HC89	16	25	0001*	
2H70	17	24	755U	
HPPO	18	23	3827	
1293	19	22	3C96	
HAP7	20	21	0000	

3C96	1	16	0001	
3827	2	15	4POA	
755U	3	14	12U3	
0000	4 U24	13	PC01	
0000	5	12	F2A6	
0001	6	11	6H49	
P255	7	10	0996	
0000	8	9	U3H5	

0000 = Ground
0001 = +5V

Notes: 1. Signatures are the same for both Rev. A and Rev. B software.
2. * = Probe is pulsing on +5V or ground signature.

8-C-45. ROM Tests (U7-U12). If the processor passes the kernel test (paragraph 8-C-44), test the ROM's as follows.

1. Connect the 5004A control Leads as indicated then check the ROM signatures. Note the change in edge trigger for START and STOP.

Clock - U5(7) - Falling edge
Start - (see Table 8-C-6) - Falling edge
Stop - (see Table 8-C-6) - Rising edge

2. Check the ROM's until at least one is found with correct signatures. If none of the ROM's are good, the problem is likely the data bus. Check each bus line for a stuck 0 or 1, or two lines shorted together.

3. If the ROM's themselves are good, reinstall A60U13 and place S1(5) in the down (open) position. Do not install A60J1 yet.

4. Connect the 5004A control leads as indicated. Note the edge change.

Table 8-C-6. ROM Test Signatures.

Note: The START/STOP connections are always together but at a different location for each ROM, as indicated.

ROM U7

Start/Stop - U24(7)

+5V = P254

GND = 0000

	Revision A					Revision B				
	9241	1		24	P254	9241	1		24	P254
	8AUC	2		23	1U5P	8AUC	2		23	1U5P
	65CA	3		22	AAHU	65CA	3		22	AAHU
	46HC	4		21	P254	46HC	4		21	P254
	C7A5	5		20	0000*	C7A5	5		20	0000*
	12UO	6	U7	19	U665	12UO	6	U7	19	U665
	3HUA	7		18	826P	3HUA	7		18	826P
	FA11	8		17	H47A	FA11	8		17	0580
	252F	9		16	6HH7	6495	9		16	7495
	H4AP	10		15	9HC6	7920	10		15	A6CP
	HA7C	11		14	C1CF	3H4A	11		14	P29U
	0000	12		13	644F	0000	12		13	5938

ROM U8

Start/Stop - U24(9)

	Revision A					Revision B				
	9241	1		24	P254	9241	1		24	P254
	8AUC	2		23	1U5P	8AUC	2		23	1U5P
	65CA	3		22	AAHU	65CA	3		22	AAHU
	46HC	4		21	P254	46HC	4		21	P254
	C7A5	5		20	0000*	C7A5	5		20	0000*
	12UO	6	U8	19	U665	12UO	6	U8	19	U665
	3HUA	7		18	826P	3HUA	7		18	826P
	FA11	8		17	83PH	FA11	8		17	3H7H
	76H3	9		16	94C7	CA53	9		16	F6UO
	3F55	10		15	F9P4	55AH	10		15	96F1
	6162	11		14	58U6	51F7	11		14	PH33
	0000	12		13	UF24	0000	12		13	736U

ROM U9

Start/Stop - U24(10)

	Revision A					Revision B				
	9241	1		24	P254	9241	1		24	P254
	8AUC	2		23	1U5P	8AUC	2		23	1U5P
	65CA	3		22	AAHU	65CA	3		22	AAHU
	46HC	4		21	P254	46HC	4		21	P254
	C7A5	5		20	0000*	C7A5	5		20	0000*
	12UO	6	U9	19	U665	12UO	6	U9	19	U665
	3HUA	7		18	826P	3HUA	7		18	826P
	FA11	8		17	3F3H	FA11	8		17	F114
	FH29	9		16	176U	AAOH	9		16	A15F
	2P17	10		15	211H	3U12	10		15	3PC6
	7A10	11		14	6516	7910	11		14	0213
	0000	12		13	76P9	0000	12		13	2511

ROM U10

Start/Stop - U24(11)

	Revision A					Revision B				
	8241	1		24	P254	9241	1		24	P254
	8AUC	2		23	1U5P	8AUC	2		23	1U5P
	65CA	3		22	AAHU	65CA	3		22	AAHU
	46HC	4		21	P254	46HC	4		21	P254
	C7A5	5		20	0000*	C7A5	5		20	0000*
	12UO	6	U10	19	U665	12UO	6	U10	19	U665
	3HUA	7		18	826P	3HUA	7		18	826P
	FA11	8		17	8CA5	FA11	8		17	066C
	H407	9		16	3008	8U69	9		16	8C18
	77UU	10		15	A05A	9UFA	10		15	2713
	93C2	11		14	7169	7C3H	11		14	451F
	0000	12		13	68C2	0000	12		13	7U19

Table 8-C-6. ROM Test Signatures (Cont'd).

	Revision A					Revision B				
	9241	1		24	P254	9241	1		24	P254
	8AUC	2		23	1U5P	8AUC	2		23	1U5P
	65CA	3		22	AAHU	65CA	3		22	AAHU
ROM U11	46HC	4		21	P254	46HC	4		21	P254
	C7A5	5		20	0000*	C7A5	5		20	0000*
	12UO	6	U11	19	U665	12UO	6	U11	19	U665
	3HUA	7		18	826P	3HUA	7		18	826P
Start/Stop - U24(12)	FA11	8		17	U5CC	FA11	8		17	C878
	4011	9		16	01UA	F447	9		16	6U12
	CA6H	10		15	39P6	C397	10		15	F592
	062A	11		14	2U10	7875	11		14	9CFO
	0000	12		13	4705	0000	12		13	F7AP

	Revision A					Revision B				
	9241	1		24	P254	9241	1		24	P254
	8AUC	2		23	1U5P	8AUC	2		23	1U5P
	65CA	3		22	AAHU	65CA	3		22	AAHU
ROM U12	46HC	4		21	P254	46HC	4		21	P254
	C7A5	5		20	0000*	C7A5	5		20	0000*
	12UO	6	U12	19	U665	12UO	6	U12	19	U665
	3HUA	7		18	826P	3HUA	7		18	826P
Start/Stop - U24(13)	FA11	8		17	CH3U	FA11	8		17	AC87
	771C	9		16	FFP7	FH6A	9		16	AC7C
	A1FP	10		15	HOC8	71AO	10		15	1F6H
	HAPC	11		14	P412	8885	11		14	7C57
	0000	12		13	C54H	0000	12		13	AAH5

Notes: 1. * = probe is pulsing on ground signature.

Clock - U5(7) - Falling edge
Start - TP4 - Rising edge
Stop - TP4 - Falling edge

5. Cycle the 3586 POWER switch. Close A60S1(1) then open it. Close A60S1(4) then open it.

6. Check the +5V signature. It should be 494P. If not, check the signatures on U2, U3, U4 and U13 (see Table 8-C-7). If they are good, replace U25 first and U26 next.

7. If any of the signatures in Table 8-C-7 are bad, replace the indicated chip. If still bad, check the associated line for shorts, opens, or two pins shorted together.

8. If the +5V signature is 494P, check the signatures on U13 pins 3,5,7,9,11,13,15 and 17. If bad, replace U13.* If the data bus signatures are good with the ROM's reconnected through U13, connect the remainder of the data bus IC's back to the bus by reinstalling shorting assembly A60J1. Now open all contacts of A60S2 (record present settings first).

9. Cycle the 3586 POWER switch. Close A60S1(1) then open it. Close A60S1(4) then open it.

10. Recheck the signatures on U13 pins 3,5,7,9,11,13,15 and 17. If any of the signatures are now bad, the problem is on the other side of J1. Trace the bad line with a current tracer if the line is shorted. If the line is not shorted, or a current tracer is not available, try pulling

* If good, check the signatures at U6 (26-33) and J1 (9-16) to verify that the traces on the PC board are good.

Table 8-C-7. ROM Data Buffer Signatures.

U2

*494P	1	14	494P
*0000	2	13	494P
------	3	12	494P*
0000	4	11	------
A710	5	10	494P*
494P	6	9	494P*
0000	7	8	0000*

U3

494P	1	14	494P
0000	2	13	494P
*0000	3	12	------
*0000	4	11	494P
*494P	5	10	494P
*0000	6	9	0000
0000	7	8	494P

U4

494P	1	14	494P
0000	2	13	0000*
494P	3	12	494P*
0000	4	11	494P*
*0000	5	10	0000*
*494P	6	9	494P*
0000	7	8	0000*

U13

*0000	1	20	494P
6FFO	2	19	0000*
6FFO	3	18	A5HH
76F6	4	17	A5HH
76F6	5	16	28C4
942F	6	15	28C4
942F	7	14	4F1P
4986	8	13	4F1P
4986	9	12	C2F8
0000	10	11	C2F8

Notes:
1. See paragraph 8-C-45.
2. +5V = 494P.
3. * = Probe is pulsing on +5V or ground signature.
4. Signatures are valid for both Rev. A and Rev. B software.

U18 out of its socket first since that's the easiest item to eliminate from consideration. If the line is still bad, find the line designator in Table 8-C-8 and replace the indicated IC's one at a time, in the order listed, until the bad component is found.

11. Close contacts 5-8 on A60S2. Check the +5V signature. It should be 1C4C. If not, check the processor (paragraph 8-C-44). If the processor is good, change U27, U36, and then U38.

Table 8-C-8. Data Bus Components.

Pin No.	Data Line	Suspect IC's
U13(9)	D0	U39, U29, U16
U13(7)	D1	U40, U29, U16
U13(5)	D2	U41, U29, U16
U13(3)	D3	U42, U29, U16
U13(11)	D4	U38, U28, U14
U13(13)	D5	U38, U28, U14
U13(15)	D6	U36, U28, U14
U13(17)	D7	U36, U28, U14

Notes:
1. Use caution in handling replacement IC's for U28 and U29 as these chips are especially sensitive to static electricity damage.
2. See paragraph 8-C-45, step 10.

8-C-46. NMOS RAM Test (U14 and U16). If the processor and the ROM's are good, test the NMOS RAM's as follows.

1. Connect the 5004A control leads as indicated.

Clock - U5(7) - Falling edge
Start - TP4 - Rising edge
Stop - TP4 - Falling edge

2. Set all contacts on A60S1 to the down (open) position. Set A60S2 contacts 5-8 as shown in Table 8-C-9 for the NMOS RAM test.

Table 8-C-9. A60S2 Test Positions.

Test	A60S2 (5)	(6)	(7)	(8)
ROM	C	C	C	C
NMOS RAM	O	C	C	C
CMOS RAM	C	O	C	C
P.I.A.	O	O	C	C
Shift Registers	C	C	O	C
Display	O	C	O	C
Keyboard	C	O	O	C

Notes: 1. C = Closed O = Open
2. Contacts 1-4 do not affect the tests.

3. Cycle the 3586 POWER switch. Close A60S1(1) then open it. Close A60S1(4) then open it.

4. Check the +5V signature. It should be P2P8. If not, check the signatures on U14, U16, U25, U26, and U27 (see Table 8-C-10).

5. If any of the signatures in Table 8-C-10 are bad, replace the associated IC. If still bad, check for shorts or opens on the affected line(s).

8-C-47. CMOS RAM Test (U28 and U29). If the processor and the ROM's are good, test the CMOS RAM's as follows.

The CMOS RAM's (A60U28 and U29) are extremely susceptible to static electricity damage. Use grounded tools and wristbands when handling loose components or working in the vicinity of in-circuit components.

1. Connect the 5004A control leads as indicated.

Clock - U5(7) - Falling edge
Start - TP4 - Rising edge
Stop - TP4 - Falling edge

2. Set all contacts on A60S1 to the down (open) position. Set A60S2 contacts 5-8 as shown in Table 8-C-9 for the CMOS RAM test.

Table 8-C-10. NMOS RAM Test Signatures.

4987	1	18	P2P8
PC48	2	17	725C
HF82	3	16	73UA
FA9F	4	15	03C7
8F32	5	14	084F
60CP	6	13	AOPP
PCCF	7	12	680C
FH09	8	11	0688
0000	9	10	P2P8*

U14

4987	1	18	P2P8
PC48	2	17	725C
HF82	3	16	73UA
FA9F	4	15	03C7
8F32	5	14	805A
60CP	6	13	549P
PCCF	7	12	31A3
FH09	8	11	9U36
0000	9	10	P2P8*

U16

7181	1	16	P2P8
7181	2	15	FH09
7181	3	14	P2P8
7181	4	13	P2P8
*0000	5	12	P2P8
64PH	6	11	P2P8
P2P8	7	10	P2P8
0000	8	9	P2P8*

U26

64U3	1	14	P2P8
FH09	2	13	0000*
FH09	3	12	0000
OA4C	4	11	0000*
*P2P8	5	10	FH09
*P2P8	6	9	861C
0000	7	8	P2P8

U25

------	1	14	P2P8
0000	2	13	8F32
64U3	3	12	6PHA
861C	4	11	60CP
OA4C	5	10	8256
P8A3	6	9	PCCF
0000	7	8	0954

U27

Notes: 1. * = Probe is pulsing on + 5V or ground signature.
2. See paragraph 8-C-46.
3. Signatures are valid for both Rev. A and Rev. B software.

3. Cycle the 3586 POWER switch. Close A60S1(1) then open it. Close A60S1(14) then open it.

4. Check the + 5V signature. It should be 61UO. If not, check the signatures on U28 and U29 per Table 8-C-11.

5. If any of the signatures in Table 8-C-11 are bad, replace the associated IC. If still bad, check for shorts or opens on the affected lines.

Table 8-C-11. CMOS RAM Test Signatures.

5UCA	1	18	61UO
40AP	2	17	589P
778U	3	16	55A5
794U	4	15	0000
C46C	5	14	77CF
UH57	6	13	31FF
AP9P	7	12	OF46
0000	8	11	1441
32C8	9	10	32C8

U28

5UCA	1	18	61UO
40AP	2	17	589P
778U	3	16	55A5
794U	4	15	0000
C46C	5	14	9728
UH57	6	13	6549
AP9P	7	12	754H
0000	8	11	7U90
32C8	9	10	32C8

U29

Notes: 1. Signatures are valid for both Rev. A and Rev. B software.
2. See paragraph 8-C-47.

8-C-48. PIA Test (U18). If the processor and the ROM's are good, test the Parallel Interface Adapter (PIA) U18, output latches U21 and U22, buffer U1, decoders U30 and U31, and gates U32 and U35 as follows.

1. Connect the 5004A control leads as indicated.

   Clock - U5(7) - Falling edge
   Start - TP4 - Rising edge
   Stop - TP4 - Falling edge

2. Set all contacts on A60S1 to the down (open) position. Set the A60S2 contacts 5-8 as shown in Table 8-C-9 for the PIA test.

3. Cycle the 3586 POWER switch. Close A60S1(1) then open it. Close A60S1(4) then open it.

4. Check the +5V signature. It should be 484F. If not, check the signatures on U1, U18, U21, U22, U30, U31, U32, and U35 per Table 8-C-12.

5. If any of the signatures in Table 8-C-12 are bad, replace the associated IC. If still bad, check for shorts or opens on the affected lines.

Table 8-C-12. PIA Test Signatures.

U1

0000	1	20	484F
74U4	2	19	0000
74U4	3	18	403P
4P2C	4	17	403P
4P2C	5	16	3486
1A94	6	15	3486
1A94	7	14	851U
1UFC	8	13	851U
1UFC	9	12	7505
0000	10	11	7505

U18 (PIA)

0000	1	40	(unstable)
1UFC	2	39	484F
7505	3	38	0000
1A94	4	37	0000
851U	5	36	2U3F
4P2C	6	35	2906
3486	7	34	484F
74U4	8	33	4373
403P	9	32	2P61
F814	10	31	P2U5
692P	11	30	635P
2H39	12	29	9A2P
50C2	13	28	U2F4
H710	14	27	541U
HH2F	15	26	A9C6
F730	16	25	484F*
51CO	17	24	484F*
(unstable)	18	23	P700
P3AP	19	22	484F*
484F	20	21	P700

U21

484F	1	20	484F
CU55	2	19	1426
4P2C	3	18	851U
3486	4	17	1A94
3808	5	16	3CUU
7HF7	6	15	2PC9
74U4	7	14	7505
403P	8	13	1UFC
H4U3	9	12	29P4
0000	10	11	PAC5

U22

484F	1	20	484F
FP70	2	19	C795
4P2C	3	18	851U
3486	4	17	1A94
3338	5	16	PFA7
CC8F	6	15	9959
74U4	7	14	7505
403P	8	13	1UFC
8AH7	9	12	UCAC
0000	10	11	9F64

Table 8-C-12. PIA Test Signatures (Cont'd).

F814	1	16	484F
692P	2	15	PH8A
2H39	3	14	3F67
0000	4	13	6UF3
P3AP	5	12	31U7
50C2	6	11	5CH3
7P03	7	10	P373
0000	8	9	6001

U30

F814	1	16	484F
692P	2	15	UC73
2H39	3	14	9F64
50C2	4	13	C3A8
P3AP	5	12	1429
484F	6	11	1F3H
PAC5	7	10	98HA
0000	8	9	2F5H

U31

6UF3	1	14	484F
278U	2	13	1429
278U	3	12	5F65
6UF3	4	11	1F3H
------	5	10	5471
0000	6	9	98HA
0000	7	8	HO96

U32

1UFC	1	14	484F
29P4	2	13	29P4
FUFU	3	12	851U
7505	4	11	6U36
29P4	5	10	29P4
09H4	6	9	1A94
0000	7	8	CH62

U35

Notes:
1. Allow time for signatures to stabilize (at least 3 seconds).
2. Signatures are valid for both Rev. A and Rev. B software.
3. * = probe is pulsing on +5V or ground signature.
4. See paragraph 8-C-48.

8-C-49. Shift Register Test (U19). If the processor, the PIA, and the ROM's are good, test the shift register U19 and output gates U33 and U34 as follows:

1. Remove the A1 and A2 boards for this test to prevent excessive relay cycling. To remove the A1 board, it is necessary to remove the front panel (see paragraph 8-C-66 for removal procedures).

2. Connect the 5004A control leads as indicated.

Clock - U5(7) - Falling edge
Start - TP4 - Rising edge
Stop - TP4 - Falling edge

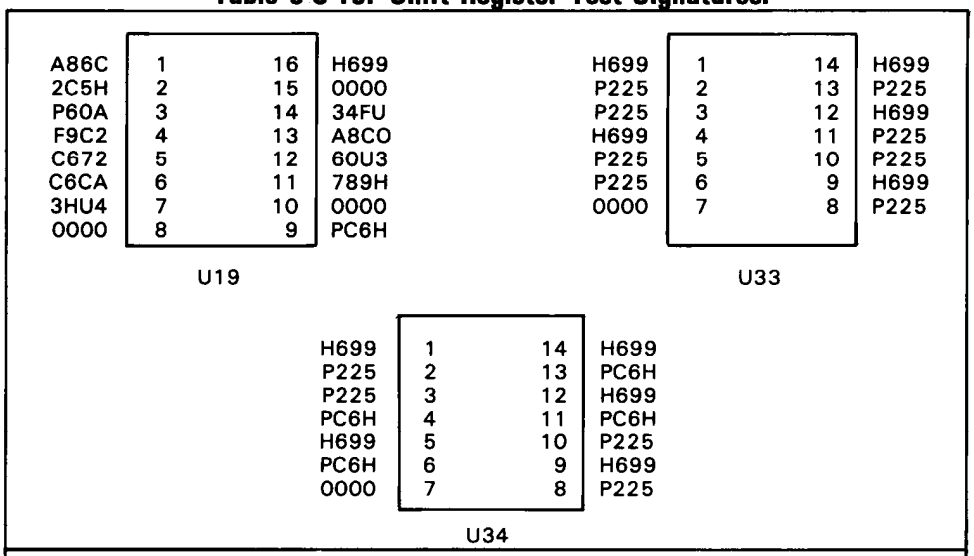
3. Set all contacts on A60S1 to the down (open) position. Set A60S2 contacts 5-8 as shown in Table 8-C-9 for the Shift Register test.

4. Cycle the 3586 POWER switch. Close A60S1(1) then open it. Close A60S1(4) then open it.

5. Check the +5V signature. It should be H699. If not, check the signatures on U19, U33, and U34 per Table 8-C-13.

6. If any of the signatures in Table 8-C-13 are bad, replace the associateed IC. If still bad, check for shorts or opens on the affected lines.

Table 8-C-13. Shift Register Test Signatures.



Notes: 1. See paragraph 8-C-49.
2. Signatures are valid for both Rev. A and Rev. B software.
3. +5V signature is H699.

8-C-50. Mnemonic Dictionary.

8-C-51. The 3586 service information contains many mnemonics that do not have either their origin or their destination on the A60 Controller board. To keep a single reference source then for all 3586 mnemonics, the mnemonic dictionary is located in the Appendix.

8-C-52. A60 Troubleshooting Hints.

8-C-53. A frozen display can be due to an inoperative display timer circuit (U20). U20 is a one-shot that gets its trigger from the processor via U18 and U31. It then outputs a display refresh timing pulse about .5 milliseconds later as an interrupt to the processor. The trigger pulse that resets U20 also is used as the display clock to gate the DSPSI data to the A98 Switch/Display shift registers. If the trigger pulse is not getting to U20(2) or U18 is not processing the interrupt at U18(40), the displays will freeze.

8-C-54. Verify that all the clock signals are present out of U5 and then check that the clock is arriving at any suspect IC. See Table 8-C-14 for clock frequencies from a typical instrument for comparison. Note they are based on a sample Controller where the 3.8MHz Oscillator circuit is running at 3.33MHz into U5(3).

Table 8-C-14. Controller Clock Frequencies.

U5 Pin	Label	Frequency	Amplitude
3	EXT	3.33MHz	3Vp-p
4	4xfo	3.8 MHz	4Vp-p
5	2xfo	1.69MHz	5Vp-p
7	BUSϕ2	845kHz	5Vp-p
9	MEM CL	845kHz	5Vp-p
13	ϕ2	845kHz	5Vp-p
15	ϕ1	845kHz	5Vp-p

Notes: 1. Frequencies and amplitudes are for comparison purposes only.

8-C-55. Test points on A60 were mostly used as development aids since there are no adjustments for the Controller board. TP1, TP2, and TP4 provide no useable troubleshooting information. TP3 is the +5V supply and may be checked for ripple with a scope. There should be no visible AC ripple on the +5V. A DVM on TP3 should show less than 5 millivolts RMS on a typical instrument.

8-C-56. Erratic processor operation or improper turn-on conditions could mean the processor is not being reset properly at turn-on. If U5(12) does not have +5.25V present with S1(1) open, either U5 or U23 are bad.

8-C-57. If the instrument won't autorange properly (or not at all), the problem could be A60U37 preventing the processor from seeing the A4 UNDERLOAD/OVERLOAD signals.

8-C-58. Switch/Display (A98) Troubleshooting.

8-C-59. The method used to troubleshoot the A98 board depends on the nature of the symptoms. If *none* of the LED's are lit, suspect a power supply problem. If *all* of the LED's are lit, suspect a processor problem. If some LED's light but others won't light, run the display check (paragraph 8-C-62) to find out which LED's won't light, then use the schematic to find out what components are common to the malfunctioning LED's. If the seven-segment displays *and* the key LED's are not working but the annunciator LED's are, suspect register U1, the display clock or the serial data input (DSPSI). If just the annunciator LED's are inoperative, suspect the appropriate latch for the group that isn't working.

8-C-60. If the displays initialize correctly at turn-on, but *none* of the key switches work, suspect a stuck switch. Run the keyboard check (paragraph 8-C-64) to find out which one. If only a couple of switches seem to be inoperative, run the keyboard check to identify *all* of the inoperative switches. If they are all common to one key line (KEY 0 - KEY 7), suspect U14. If they are all common to one vertical column of switches as shown on the schematic (Figure 8-C-7), suspect U12 or U13.

8-C-61. If the RPG is not working properly (or at all), look at KEY 6 and KEY 7 on A60U36 (put A60 on extender boards) while turning the RPG. Looking at the lines here first is easier than removing the front panel. Only the KEY 7 line should pulse HIGH when the RPG is turned CCW. When the RPG is turned CW, both KEY 6 *and* KEY 7 lines should pulse HIGH. If they do pulse correctly, the problem must be on the Controller board, possibly A60U36. If the pulses are not present at the input to A60U36, remove the front panel (see paragraph 8-C-66) and trace the KEY 6 and Key 7 lines for pulses back to the RPG until the problem is found.

8-C-62. Display Check.

8-C-63. If the instrument microprocessor is functional as indicated by successful completion of the turn-on and calibration cycle, it is possible to examine all the front panel LED's for defects by performing the following procedure.

1. Set the POWER switch to STBY. Remove the A60 board. Record the switch positions of A60S1 and A60S2 for resetting at the test conclusion.

2. Change the following contacts of A60S2 to the indicated positions:

Contact 5 - open
Contact 6 - closed
Contact 7 - open
Contact 8 - closed

3. Insert the A60 board and set the POWER switch to ON.

4. After the turn-on cycle, close contact 4 of A60S1 (pull the contact towards the top of the board) and then open it.

5. The Display test cycle will now begin. The test automatically repeats itself until manually terminated. The following events occur in the listed order:

   a. All the LED's are lit for approximately two seconds.

   b. The 7-segment LED's come on, one at a time, moving from right to left across the display. (All other LED's will be off.)

   c. The LED's in the keys of the FREQUENCY TUNE and BANDWIDTH blocks, and the MEAS CONT key turn on and then off.

   d. The LED's in the keys of the FREQUENCY/ENTRY block and the OFFSET ON-OFF key turn on and then off

   e. The LED's in the following key groups will turn on and then off, one group at a time.

      (1). RANGE; FULL SCALE; AVE; UNIT.

      (2). AUTO CAL; WIDEBAND; Shift; SELECTIVE; SSB CHANNEL.

      (3). TERMINATION (All the impedance keys).

   f. Groups of annunciators in the MEASUREMENT/ENTRY, FREQUENCY/ENTRY, and STATUS blocks turn on and then off in eight steps.

   g. All the LED's are turned on and the whole cycle starts over.

6. To exit this test procedure, set the POWER switch to STBY. Remove the A60 board, reset the switches and reinstall the board.

8-C-64. Keyboard Check.

8-C-65. If the instrument microprocessor is functional as indicated by successful completion of the turn-on and calibration cycle, it is possible to verify that each front panel key generates the correct key code when depressed. At the same time, intermittent operation of the individual keys may also be determined by multiple switch depressions. To check keyboard operation, perform the following procedure.

1. Set the POWER switch to STBY. Remove the A60 board. Record the switch positions of A60S1 and A60S2 for resetting at the test conclusion.

2. Change the following contacts of A60S2 to the indicated positions:

   Contact 5 - closed
   Contact 6 - open
   Contact 7 - open
   Contact 8 - closed

3. Insert the A60 board and set the POWER switch to ON.

4. After the turn-on cycle, close contact 4 of A60S1 (pull the contact towards the top of the board) and then open it.

5. Each key on the front panel can now be pressed, causing a different key code number to be displayed in the far right-hand portion of the FREQUENCY/ENTRY block. Refer to Table 8-C-15 to find the correct key code for a given key.

6. To exit this test procedure, set the POWER switch to STBY. Remove the A60 board, reset the switches and reinstall the board.

Table 8-C-15. Key Codes

Switch Group	Key Label	Key Code
MEASUREMENT/ENTRY	AUTO CAL OFF-ON	25
	10dB	26
	100dB	56
	AUTO	66
	ENTRY	76
	AVE	36
	dBm	46
	dBpW	16
	dB .775V	06
	OFFSET OFF-ON	07
FREQUENCY/ENTRY	CARRIER	47
	TONE	37
	◺ (LSB)	77
	◿ (USB)	67
	COUNTER OFF-ON	57
STATUS	LOCAL	27
MEASUREMENT MODE (3586A/B)	WIDEBAND	55
	FUNCTION (BLUE)	65
	LO NOISE	75
	Ø JITTER	35
	NOISE/TONE	45
	IMPULSE	15
	START	05
MEASUREMENT MODE (3586C)	WIDEBAND	55
	LO DIST	65
	LO NOISE	75
TERMINATION (3586A)	10KΩ||50pF	23
	75Ω	53
	150Ω	63
	BRIDGED	33
	600Ω	43
TERMINATION (3586B)	10KΩ||50pF	23
	75Ω	53
	124Ω	63
	135Ω	73
	BRIDGED	33
	600Ω	43

Table 8-C-15. Key Codes (Cont'd).

Switch Group	Key Label	Key Code
TERMINATION (3586C)	50Ω	23
	75Ω	53
	FUNCTION (HIGH Z)	63
	BRIDGED	33
	600Ω	43
ENTRY	FREQ	03
	FULL SCALE	13
	STORE	20
	THSHLD	21
	FREQ STEP	02
	OFFSET	22
	RECALL	50
	TIME	51
	0	61
	1	60
	2	70
	3	30
	4	52
	5	62
	6	72
	7	12
	8	42
	9	32
	• (decimal)	71
	UP (arrow)	31
	DOWN (arrow)	41
	MHz/ – dB	00
	kHz/ + dB	10
	Hz/MIN	40
	MEAS CONT	04
	RDNG → OFFSET	01
	CNTR → FREQ	11
FREQUENCY TUNE	OFF	14
	AUTO	44
	FREQ STEP	34
	RPG (CW)	90
	RPG (CCW)	91
BANDWIDTH	20Hz	74
	400Hz	64
	3100/2000/1740Hz	54
	WTD 3100Hz	24

8-C-66. Front Panel Removal.

8-C-67. For access to the A98 board for troubleshooting, the front panel must be removed using the following procedure.

1. Turn the instrument off and unplug the line cord.

2. Remove the "beauty strip" along the top front edge of the instrument. The strip simply pulls out.

3. Remove the top cover.

4. Remove the front panel assembly (front panel plus A98 keyboard) by doing the following:

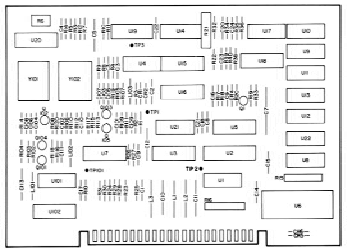
a. Remove the 8 screws holding the front panel assembly to the instrument. There are four screws along the top front edge of the instrument, and four along the bottom front edge.

NOTE

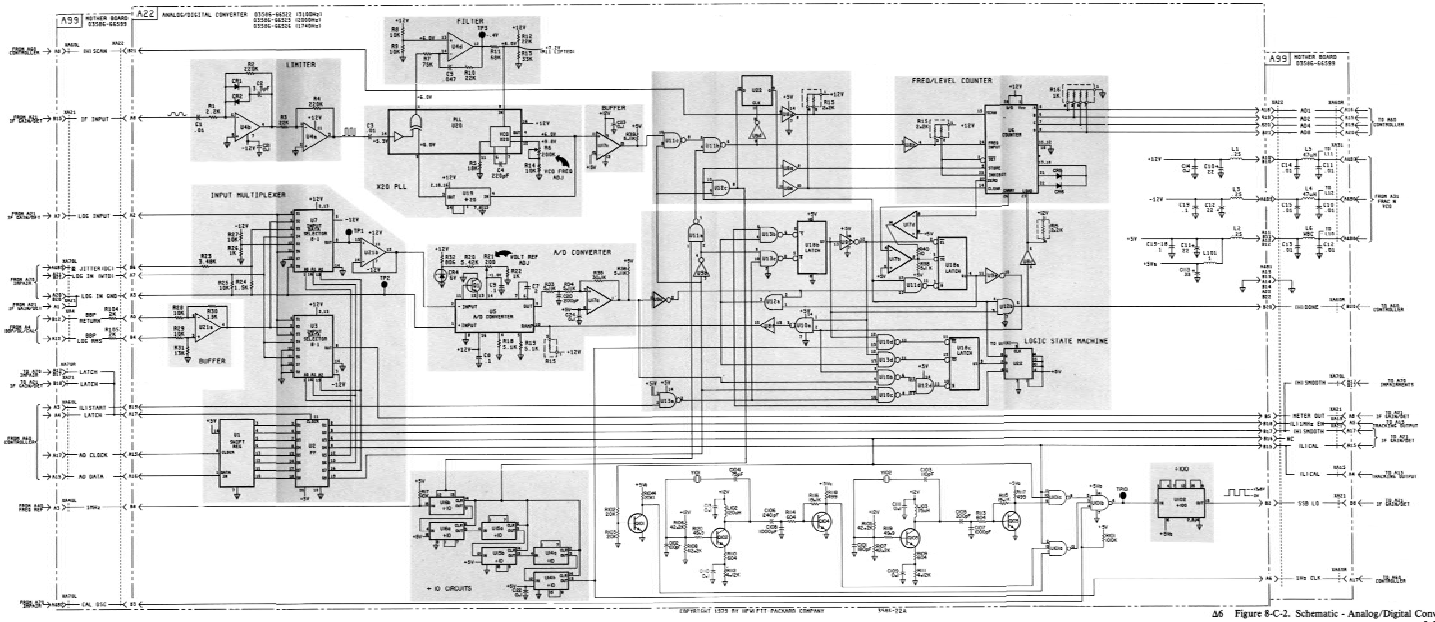
The 7 short screws (Part No. 0515-0080) go in the 4 top holes and the 3 right-hand holes on the bottom. The single long screw (Part No. 0515-0082) goes in the far left-hand hole along the bottom. These are metric screws.

b. Slowly pull the front panel assembly out of the instrument about two inches. Then unplug the two cable assemblies attached to the back of the A98 Keyboard. These are the blue ribbon cable between the A98 and A60 controller assemblies, and the brown connector of the cable between the A98 and A99 motherboard.

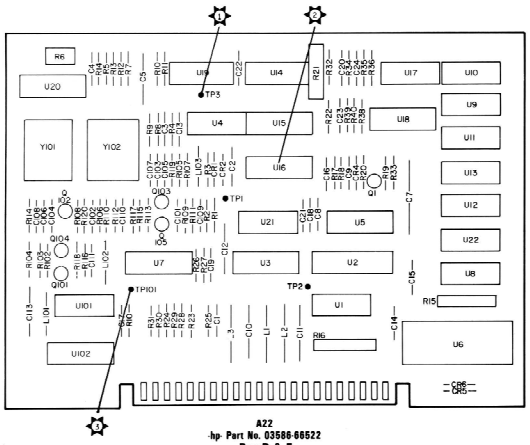
c. Remove the front panel assembly completely from the instrument. Lay the front panel assembly face down on a surface that won't scratch the front panel.



A22
-hp- Part No. 03586-66522
Rev D and E



Δ6 Figure 8-C-2. Schematic - Analog/Digital Converter (A22)
8-C-27/8-C-28



NOTES:

1. Measurements taken with 3586 set to LO DIST, ENTRY 100, Full Scale = ØdBm, tuned frequency = 1MHz, input signal = 1MHz at ØdBm.
2. Voltages shown for TP1 are valid for LO DIST (IF LOG), LO NOISE (IF LOG), WIDEBAND (BBP LOG RMS), and WTD 3100Hz (WTD LOG). Voltages at TP1 for phase jitter are the same as those shown at U7(6).
3. ERR-7 on front panel means a positive voltage is presented to the A/D (U5).

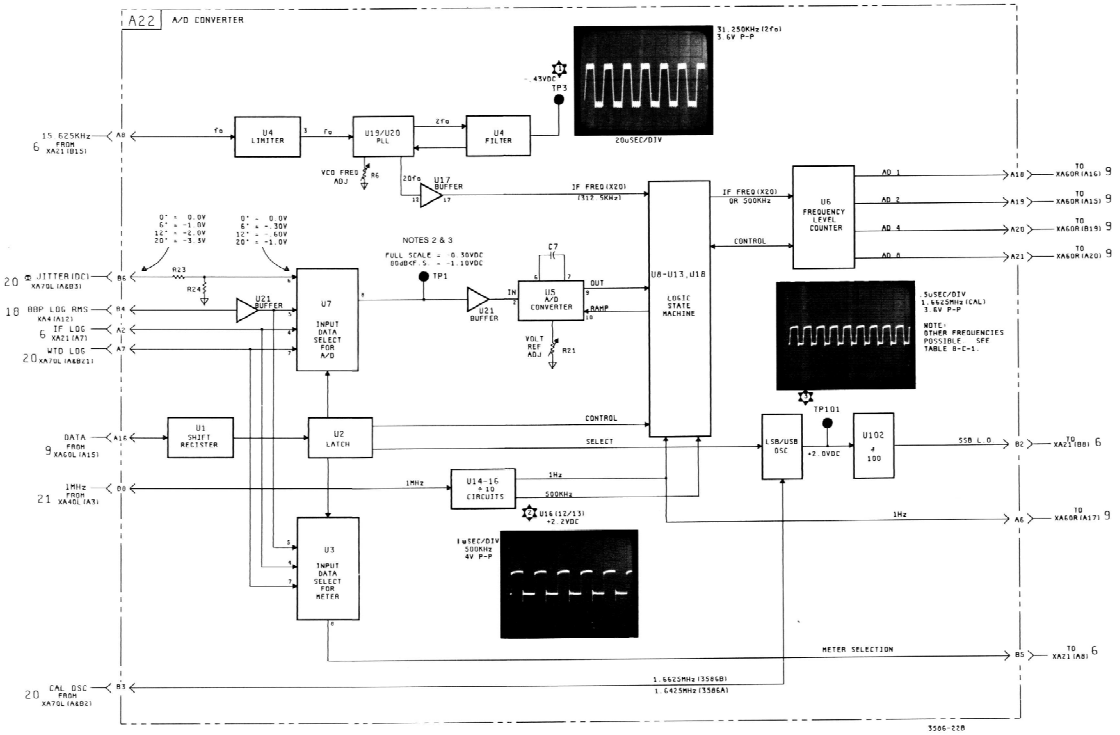
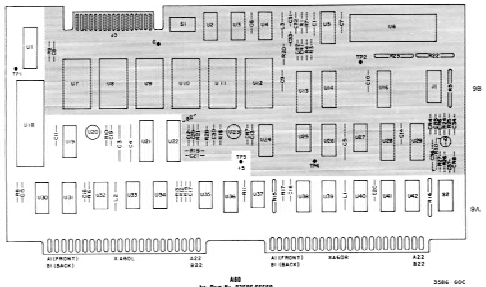
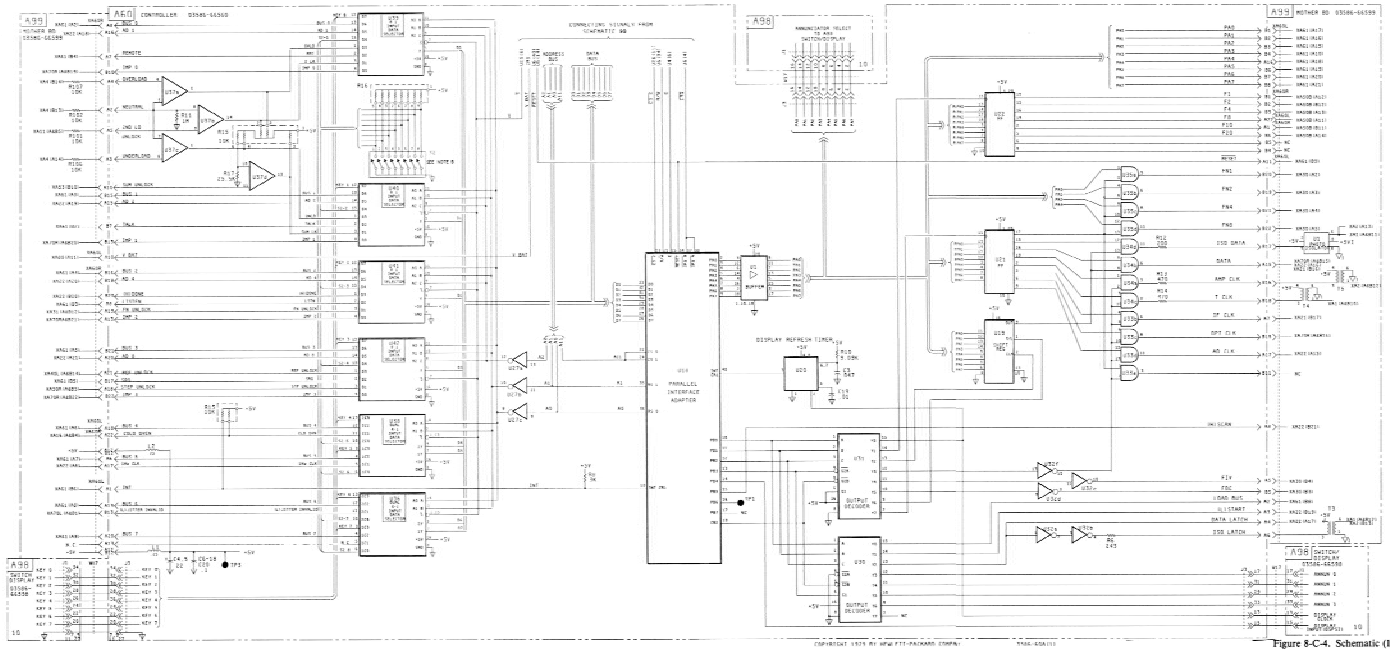


Figure 8-C-3. Functional Block - Analog/Digital Converter (A22)



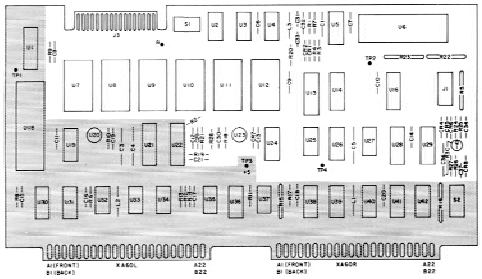
A60
Ap- Part No. 03586-66560
Rev A

NOTES:
1. U15 and U17 are not normally installed (NNI).
2. STORE/RECALL memory provided by U28 and U29 is protected when AC power is removed by application of + 2.5VDC (V BAT) from a NI-CAD battery (A60BT1).
3. Note deleted.
4. Jumper position is II for INTEL ROM's and T for Texas Instruments EPROM's. Use T position for SYNERTEK ROM's.
5. See Table 8-C-3 for settings.



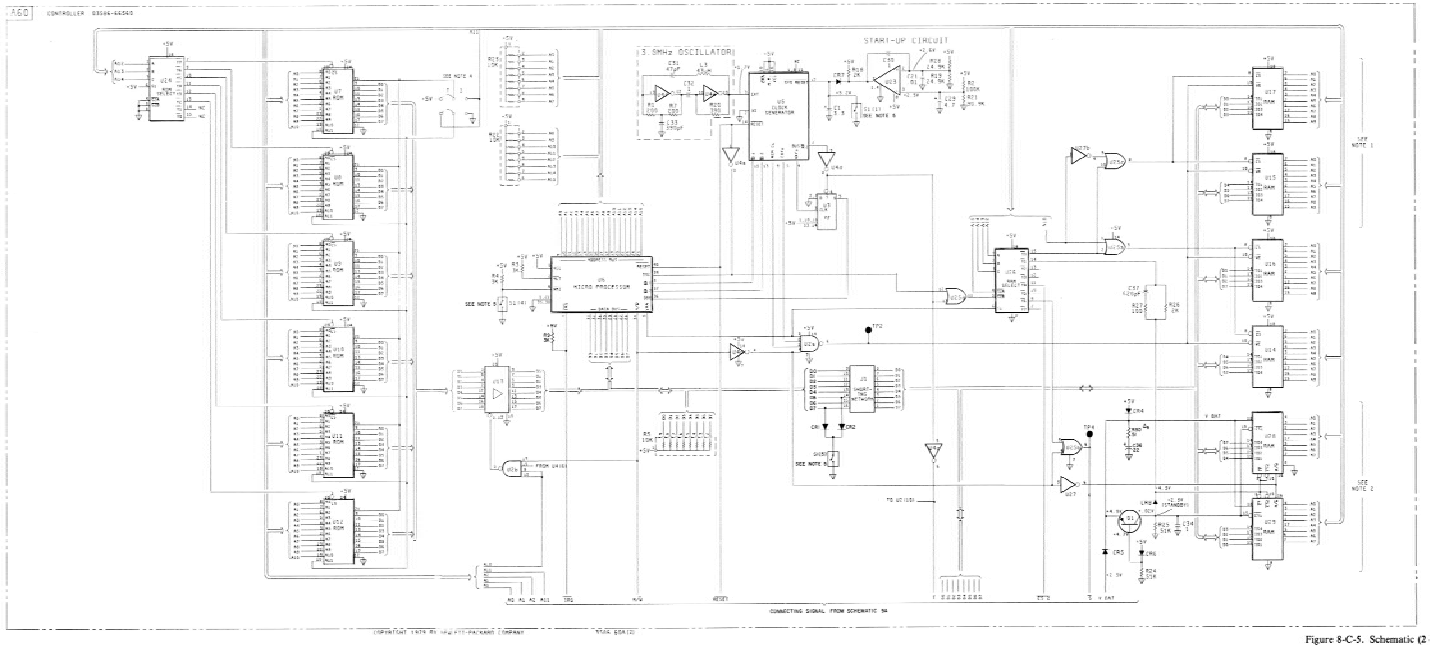
9A

Figure 8-C-4. Schematic (1 of 2) - Controller (A60)



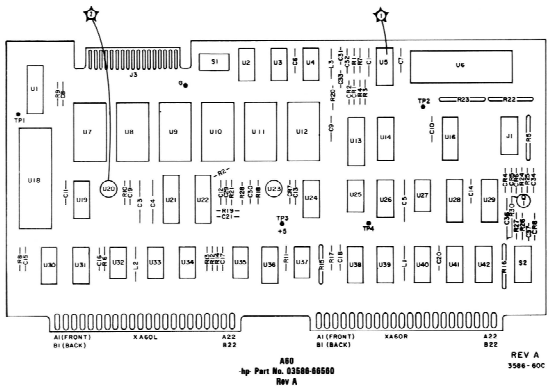
NOTES:

1. U15 and U17 are not normally installed (NNI).
2. STORE/RECALL memory provided by U28 and U29 is protected when AC power is removed by application of +2.5VDC (V-BAT) from a NI-CAD battery (A60BT1).
3. Note deleted.
4. Jumper position is I for INTEL ROM's and T for Texas Instruments EPROM's. Use T position for SYNERTEK ROM's.
5. See Table 8-C-2.



9B

Figure 8-C-5. Schematic (2 of 2) - Controller (A60)



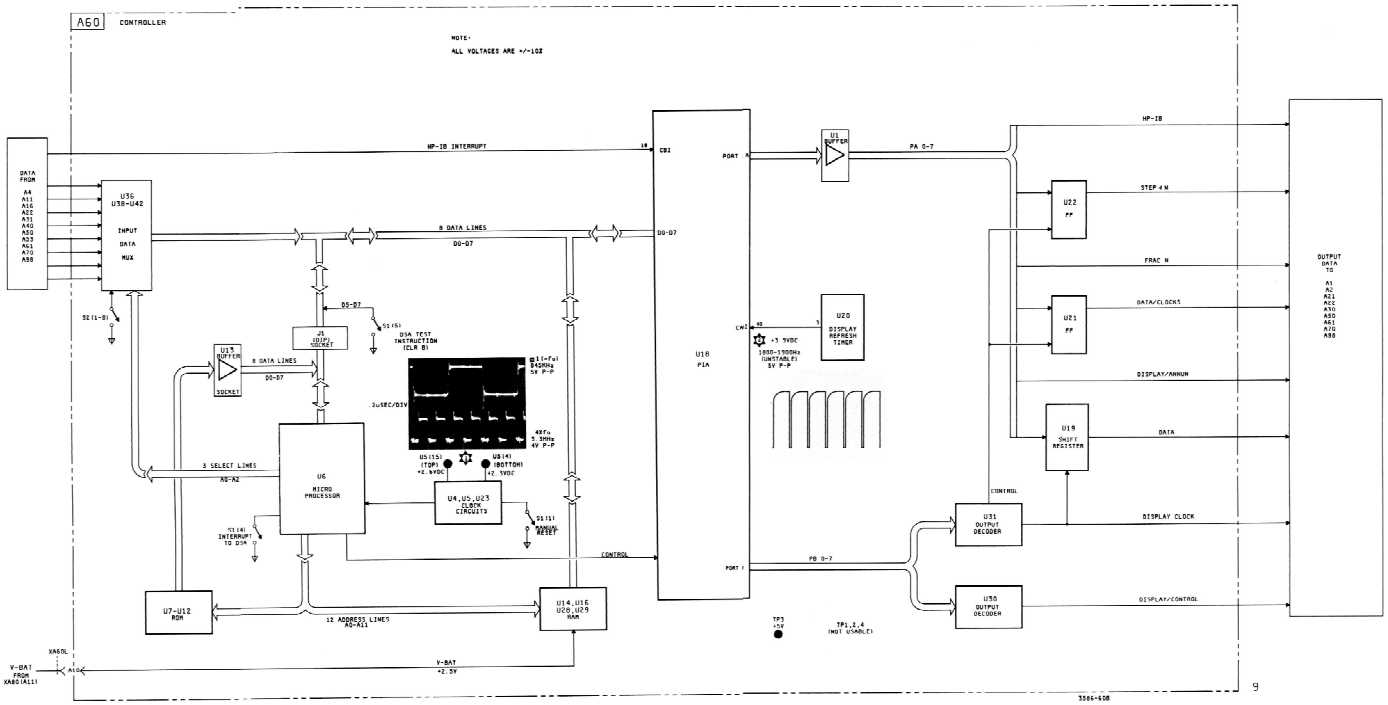
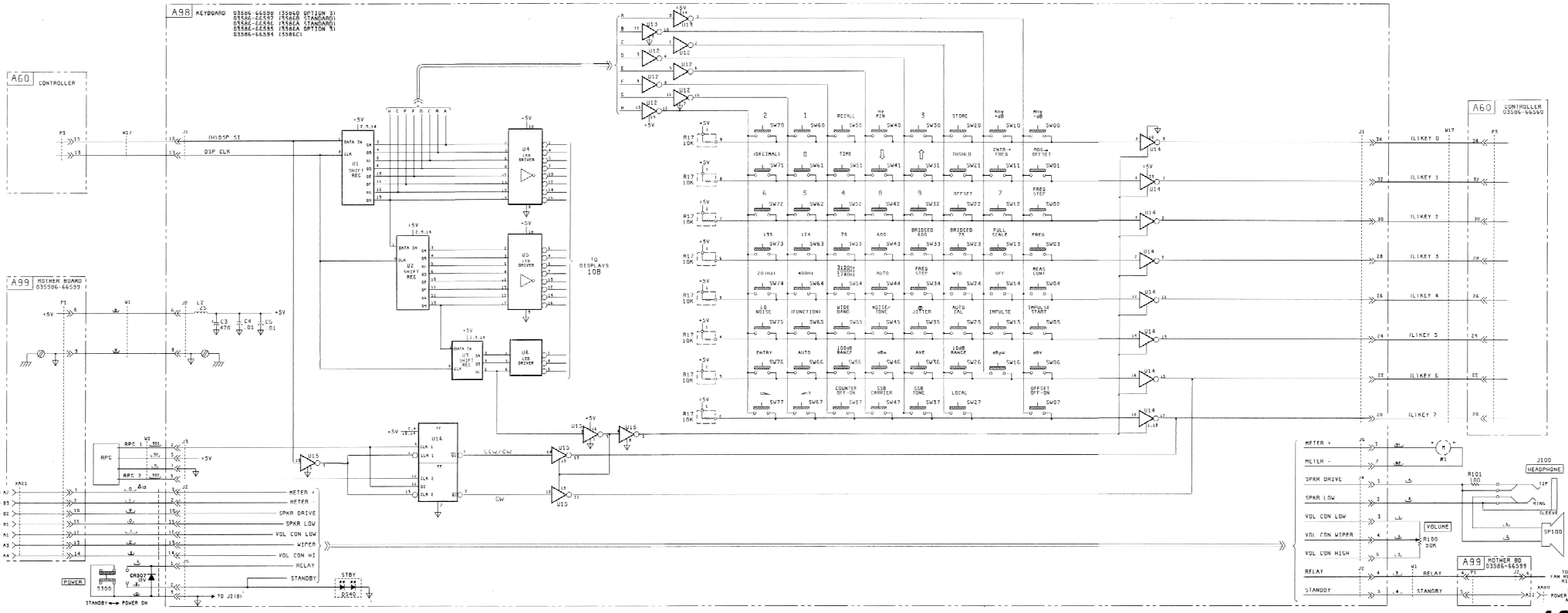
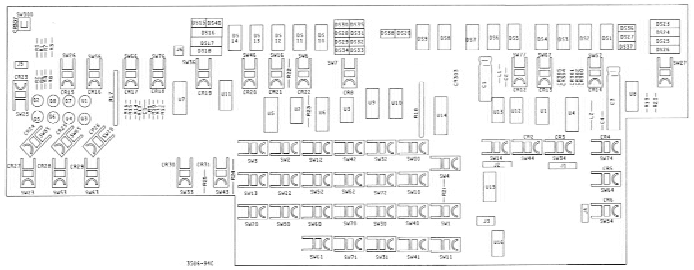


Figure 8-C-6. Functional Block - Controller (A60)

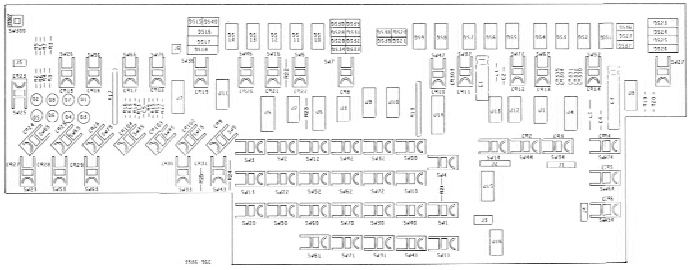


10A

Figure 8-C-7. Schematic (1 of 2) - Switch/Display (A98)



ASS
-hp- Part No. 03586-66594
Rev C



ASS
-hp- Part No. 03586-66596
Rev C

"NOTE"

03586A/B/C instruments contain front-panel pushbutton switches (P/N 5060-9436) which may be susceptible to failure. This "failure" is the tendency for the steel strip fused as a detent spring) to either crease or pop out. In either case, the switch must be replaced. Not all switches with this P/N are prone to this type of failure and there are two ways to determine if one will eventually fail. Referring to Figure 1, switches that are susceptible to failure can be identified by a series of one to three dots with NO number in the area designated "DOT LOCATION." Also, these instruments will have no visible gate mark in the area shown in Figure 2. Switches that are NOT susceptible to failure are identified as having one dot AND a number in the dot location area, plus a WHITISH gate mark in the center of the surface opposite the spring (Figure 2). If upon inspection the majority of the switches on the ASS Board are found to be failure prone, it may be more economical to replace the entire assembly.

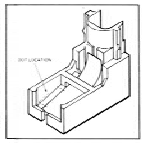


Figure 1. Pushbutton Front-Panel Switch, HP P/N 5060-9436, Mold Mark I.D.

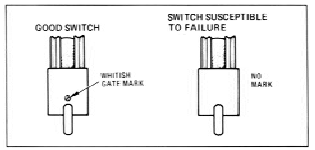
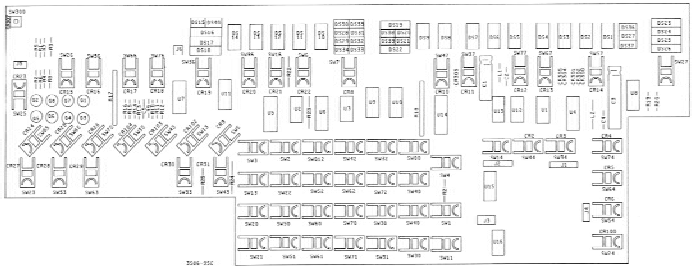
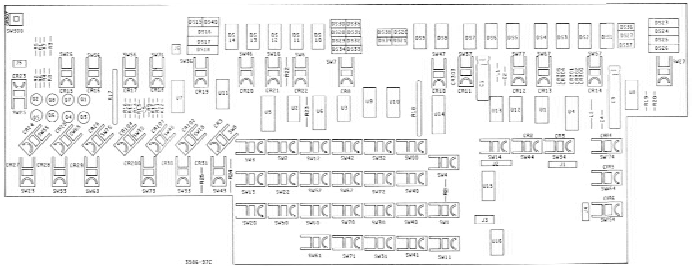


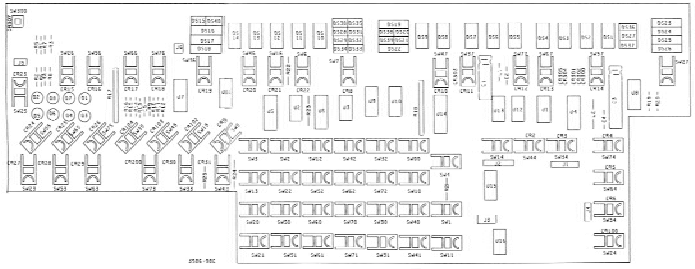
Figure 2. Pushbutton Front-Panel Switch, HP P/N 5060-9436 Gate Mark I.D.



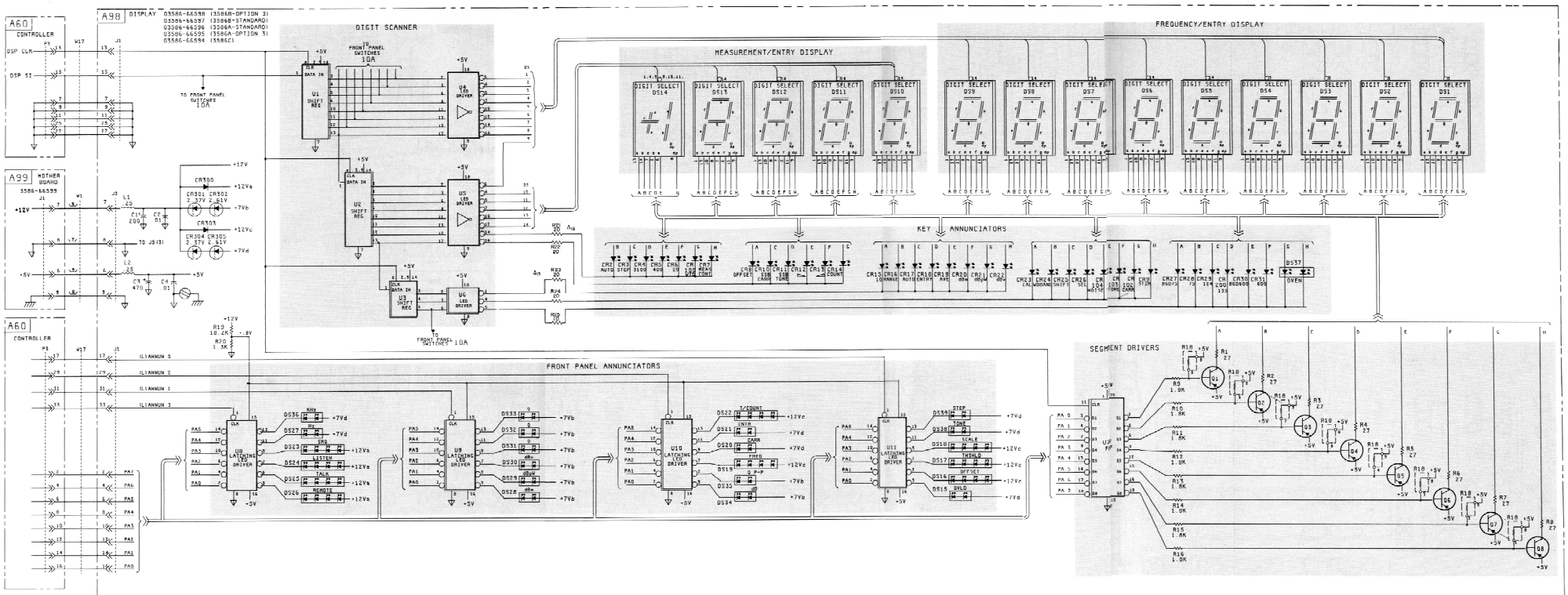
ASS
-hp- Part No. 03586-66595
Rev C



ASS
-hp- Part No. 03586-66597
Rev C

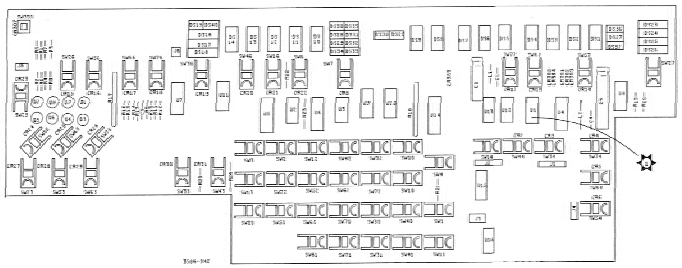


ASS
-hp- Part No. 03586-66598
Rev C

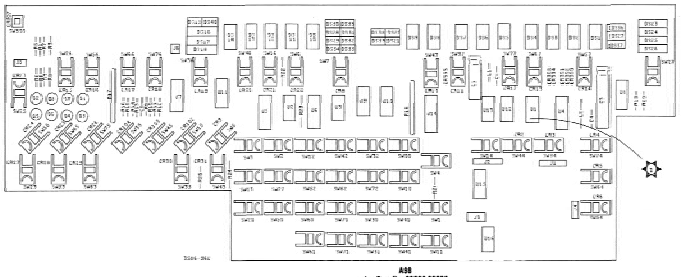


10B

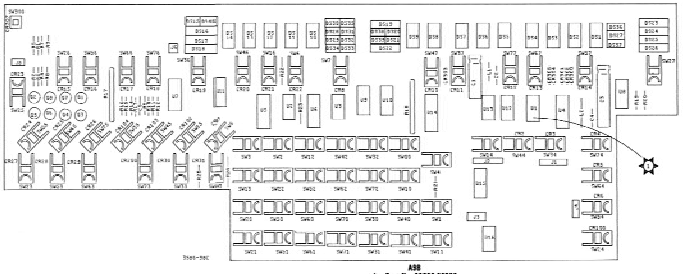
Figure 8-C-8. Schematic (2 of 2) - Switch/Display (A98)



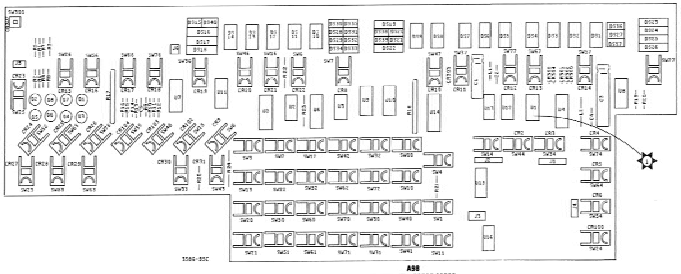
A9B
-hp- Part No. 03586-66594
Rev C



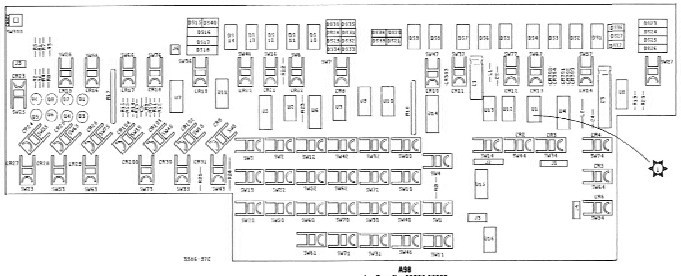
A9B
-hp- Part No. 03586-66596
Rev C



A9B
-hp- Part No. 03586-66598
Rev C



A9B
-hp- Part No. 03586-66595
Rev C



A9B
-hp- Part No. 03586-66597
Rev C

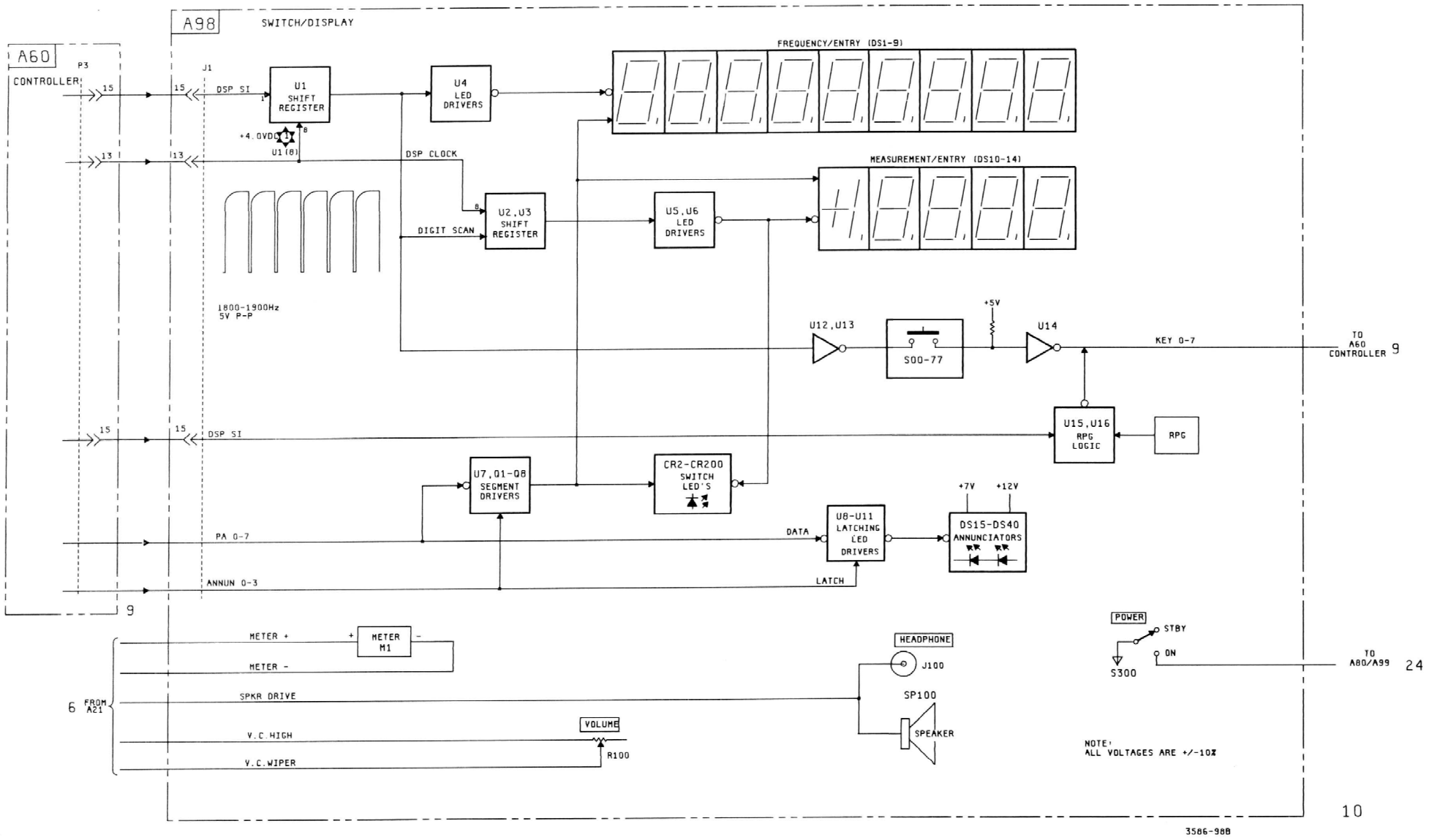


Figure 8-C-9. Functional Block -Switch/Display (A98)

Table of Contents

STEP/SUM LOOPS
SERVICE GROUP D

Contents

8-D-1. ADJUSTMENTS (CROSS REFERENCE).

8-D-2. Step Loop Adjustments (A50).

Designation	Adjustment Title	Paragraph
A50L5	Frequency Adjust	5-6
A50R45	Flatness Adjust	5-6
A50R46	Gain Adjust	5-6

8-D-3. Sum Loop Adjustments (A51/A53).

Designation	Adjustment Title	Paragraph
A51L8	Frequency Cal Adjust	5-6
A51R55	Flatness Adjust	5-6
A51R56	Gain Adjust	5-6
A53R3	Gain Adjust	5-6
A53R13	Offset Adjust	5-6

8-D-4. THEORY OF OPERATION (CROSS REFERENCE).

8-D-5. First Local Oscillator - Paragraph 8-197.

8-D-6. Step Loop (A50) - Paragraph 8-199.

8-D-7. Sum Loop VCO (A51) - Paragraph 8-212.

8-D-8. Sum Loop Mixer (A52) - Paragraph 214.

8-D-9. Sum Loop Phase Detector (A53) - Paragraph 8-216.

8-D-10. TROUBLESHOOTING DATA.

8-D-11. First Local Oscillator Troubleshooting.

8-D-12. The First L.O. can have several different problems. It can have low amplitude, incorrect frequency, or be missing completely. It can also have spurs present or sufficient phase noise present to raise the overall noise floor of the instrument out of specification. Refer to Figures 8-D-1 and 8-D-2 as necessary during the following paragraphs.

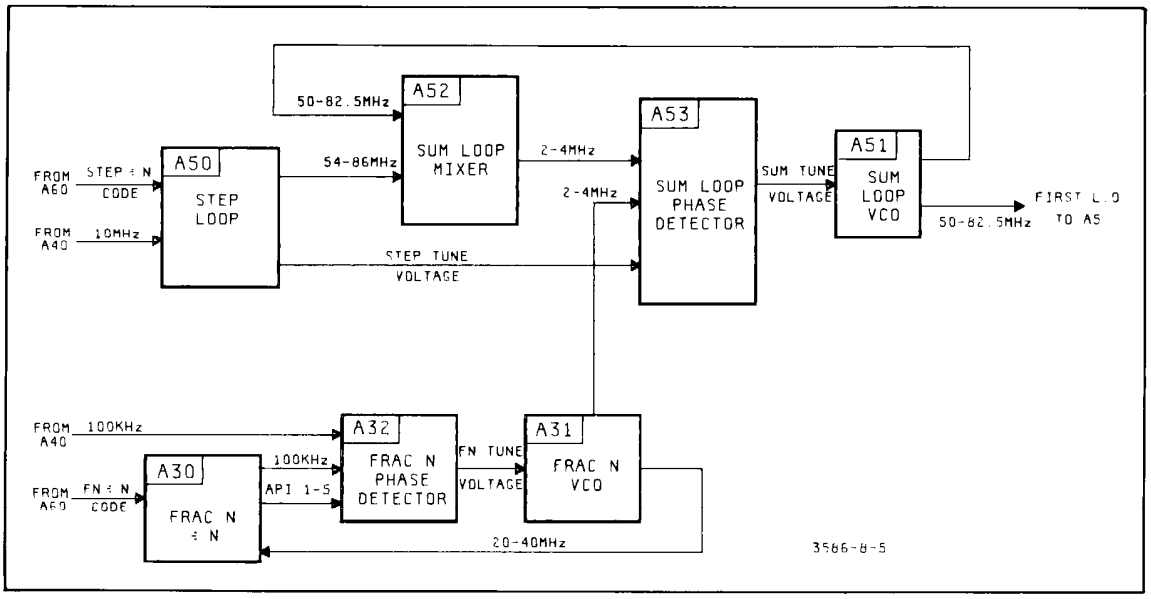


Figure 8-D-1. First Local Oscillator.

8-D-13. First L.O. Signal Missing. The First L.O. signal to the Input Mixer (A5) is a direct output of the Sum Loop VCO. If it is missing or low in amplitude, check A51J2 and A51J3 for the same signal. If present, and the sum loop is unlocked (E3.2 error code displayed and LED on A53 lit), suspect A51Q9. If the sum loop is not unlocked, suspect A51Q7 and Q8. If the signal is absent at A51J2 and J3 also, troubleshoot the sum loop (paragraph 8-D-21).

8-D-14. First L.O. Off Frequency. If the First L.O. signal is the wrong frequency as determined by the procedure in steps 3-5 under "Frequency Measurements Incorrect" in Table 8-9, proceed as follows.

1. Disconnect the red coax from A40J1 and connect it to A51J2. Connect a counter to the "EXT REF-INPUT" BNC connector on the rear panel. Press RECALL and Ø.

2. The counter should read 51MHz (tuned frequency plus 50MHz). If it does, and the tracking output BNC on the rear panel labeled "Fo(0-32MHz)" does not read 1MHz, the problem is in the tracking output circuits. Proceed to Service Group F and troubleshoot the A15 board.

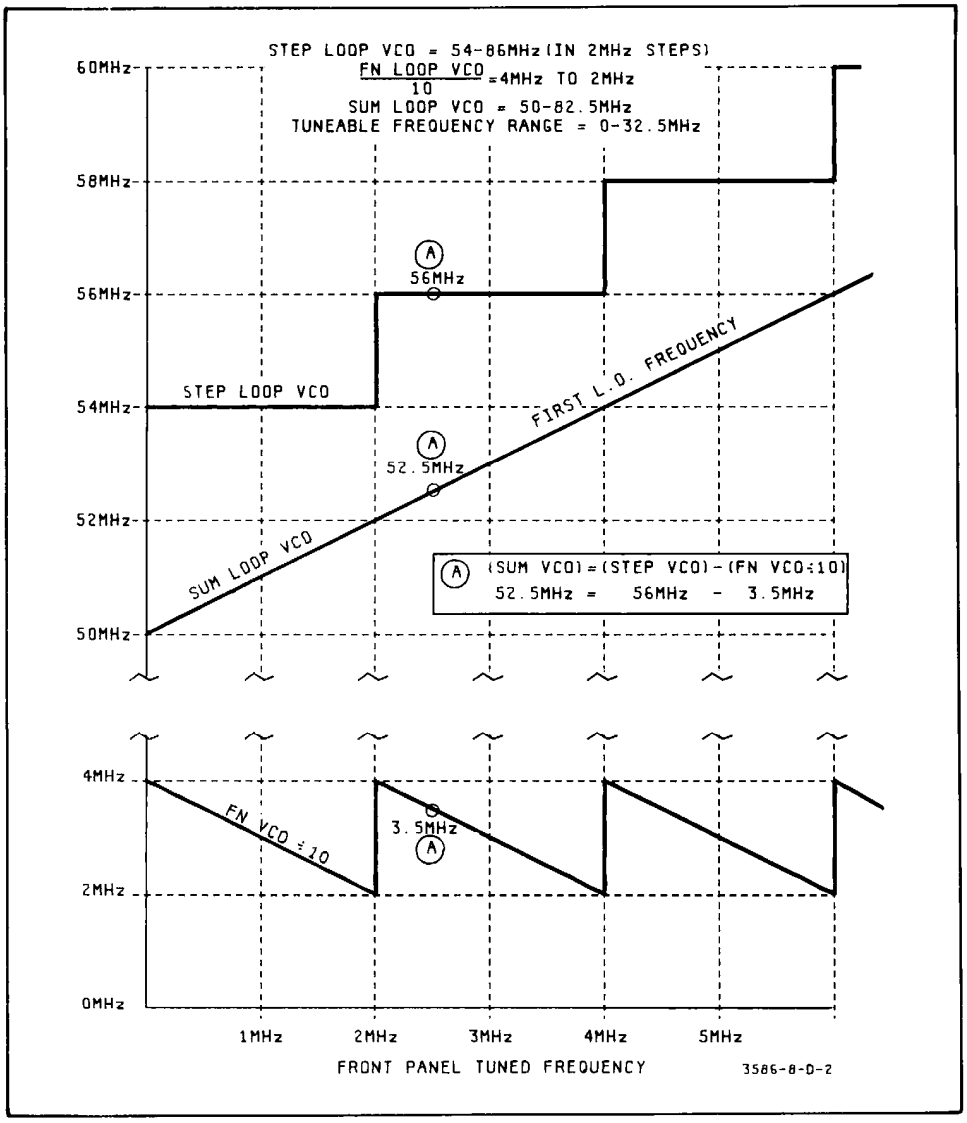


Figure 8-D-2. First L.O. Loop Relationships.

3. If the counter does not read 51MHz at A51J2, move the red coax to A50J2. The counter should now read 54MHz. If it does not, troubleshoot the step loop (paragraph 8-D-17). If it does read 54MHz, move the red coax to A31TP1. The counter should now read 30MHz. If it does not, troubleshoot the Fractional-N loop (Service Group E). If it does read 30MHz, troubleshoot the sum loop (paragraph 8-D-21).

4. If the First L.O. frequency problem occurs at some tuned frequency other than 1MHz (RECALL/Ø frequency setting), use Table 8-D-1 to determine what the correct loop frequencies should be for the tuned frequency(ies) where the problem occurs. This should identify the faulty loop.

5. Note also that in measurement modes other than LO DIST and LO NOISE, some frequency shift may normally occur between what the front panel tuned frequency reads and what the First L.O. frequency should be. In Table 8-D-2, this relationship can be clearly seen. Add 50MHz to the indicated Tracking Output Frequency to determine what the First L.O. Frequency should be for the selected mode.

Table 8-D-1. First L.O. Loop Frequencies.

Front Panel Tuned Frequency	Step Loop VCO Frequency - A50J2	Fractional-N Loop VCO Frequency (+10) - A31TP1	Sum Loop VCO Frequency (First L.O. Frequency) - A51J2
0 Hz- 1,999,999.9Hz	54MHz	4.0MHz-2,000,000.1Hz	50.0MHz-51,999,999.9Hz
2.0MHz- 3,999,999.9Hz	56MHz	4.0MHz-2,000,000.1Hz	52.0MHz-53,999,999.9Hz
4.0MHz- 5,999,999.9Hz	58MHz	4.0MHz-2,000,000.1Hz	54.0MHz-55,999,999.9Hz
6.0MHz- 7,999,999.9Hz	60MHz	4.0MHz-2,000,000.1Hz	56.0MHz-57,999,999.9Hz
8.0MHz- 9,999,999.9Hz	62MHz	4.0MHz-2,000,000.1Hz	58.0MHz-59,999,999.9Hz
10.0MHz-11,999,999.9Hz	64MHz	4.0MHz-2,000,000.1Hz	60.0MHz-61,999,999.9Hz
12.0MHz-13,999,999.9Hz	66MHz	4.0MHz-2,000,000.1Hz	62.0MHz-63,999,999.9Hz
14.0MHz-15,999,999.9Hz	68MHz	4.0MHz-2,000,000.1Hz	64.0MHz-65,999,999.9Hz
16.0MHz-17,999,999.9Hz	70MHz	4.0MHz-2,000,000.1Hz	66.0MHz-67,999,999.9Hz
18.0MHz-19,999,999.9Hz	72MHz	4.0MHz-2,000,000.1Hz	68.0MHz-69,999,999.9Hz
20.0MHz-21,999,999.9Hz	74MHz	4.0MHz-2,000,000.1Hz	70.0MHz-71,999,999.9Hz
22.0MHz-23,999,999.9Hz	76MHz	4.0MHz-2,000,000.1Hz	72.0MHz-73,999,999.9Hz
24.0MHz-25,999,999.9Hz	78MHz	4.0MHz-2,000,000.1Hz	74.0MHz-75,999,999.9Hz
26.0MHz-27,999,999.9Hz	80MHz	4.0MHz-2,000,000.1Hz	76.0MHz-77,999,999.9Hz
28.0MHz-29,999,999.9Hz	82MHz	4.0MHz-2,000,000.1Hz	78.0MHz-79,999,999.9Hz
30.0MHz-31,999,999.9Hz	84MHz	4.0MHz-2,000,000.1Hz	80.0MHz-81,999,999.9Hz
32.0MHz-32,500,000.0Hz	86MHz	4.0MHz-3,500,000.0Hz	82.0MHz-82,500,000.0Hz

NOTES: 1. These frequencies are valid for LO DIST and LO NOISE modes only. See Table 8-D-2 for First L.O. frequency shifts in other operating modes.

Table 8-D-2. Tracking Output Frequencies vs. Mode Selections.

Measurement Mode Selection	Entry Frequency	Channel	Tracking Output Frequency #
LO DIST, LO NOISE, WIDEBAND	*	*	1,000,000Hz
NOISE/DEMOD, NOISE/TONE, PHASE JITTER, IMPULSE	CARRIER	↗	1,001,850Hz
	CARRIER	↘	998,150Hz
	TONE	↘	999,154Hz (998,950Hz)
	TONE	↗	1,000,846Hz (1,001,050Hz)
TONE 1004Hz (TONE 800Hz) #	TONE	*	1,000,000Hz
	CARRIER	↘	998,996Hz (999,200Hz)
	CARRIER	↗	1,001,004Hz (1,000,800Hz)
CARRIER	CARRIER	*	1,000,000Hz
	TONE	↘	1,001,004Hz (1,000,800Hz)
	TONE	↗	998,996Hz (999,200Hz)
SIGNAL 2600Hz (1010Hz) #	TONE	↗	1,001,596Hz (1,000,210Hz)
	TONE	↘	998,404Hz (999,790Hz)
	CARRIER	↘	997,400Hz (998,990Hz)
	CARRIER	↗	1,002,600Hz (1,001,010Hz)

NOTES: 1. All readings taken with front panel tuned frequency = 1,000,000Hz.
2. # Where only one frequency is given, applies to 3586A/B. Where two frequencies given, first = 3586B, second ( ) = 3586A.
3. * Selection has no effect on T. O. frequency.

8-D-15. Spurious Signals. When spurs are found to be riding on the First L.O. signal, a spectrum analyzer such as the 3585A is the best troubleshooting aid since there are seven boards (A50-A53, and A30-A32) and three loops (step, sum and fractional-N) making up the First L.O. signal. Using Figures 8-D-4, 8-D-8, and 8-E-6, check for spurs at all key test points. The following information may also help.

1. Note that residual spurs (no input signal) are specified to be less than −115dBm (in the 20Hz bandwidth) for all frequencies above 300Hz *and less than −100dBm for all frequencies below 300Hz.*

2. 60Hz (or multiples thereof) inside the 3586 can enter through the step loop supply voltages and get into the sum loop at the A52 mixer stage.

3. Both A50 and A51 must be screwed down tight to prevent signals from either board mixing with signals on the other board to cause spurs. Look especially for spurs at the difference frequency (i.e., step-sum = spur) which could be riding the Sum VCO output. For example, if the Step = 60MHz and the Sum = 57.5MHz (front panel tuned frequency = 7.5MHz), spurs could occur at 5MHz and 10MHz (60 - 57.5MHz = 2.5MHz, 7.5MHz ± 2.5MHz).

4. If spurs are noted at specific frequencies close to the tuned frequency, determine the theoretical difference frequency and try to identify the source. For example, if the tuned frequency is 2.3MHz and a spur is noted at 2.300120MHz, look for high ripple on a DC supply voltage since the difference frequency is 120Hz and could be a harmonic of the line frequency.

5. Also, spurs that form sidebands on the L.O. of about 100 ± 10Hz could be due to the Display Scan Rate (see paragraphs 8-78 and 8-266) somehow getting into the First L.O. signal.

6. Spurs of exactly 2MHz could be related to the A50 board since the step loop uses a reference frequency of exactly 2MHz.

7. Refer to Table 8-D-3 for a list of frequencies normally occurring on PC boards in the 3586 for identifying possible spurious signal sources.

8. Remember that any amplifier stage is capable of breaking into oscillation if a positive feedback path is provided. Failure of clamping diodes, leaky capacitors, etc. can sometimes provide that path. With no input signal to the 3586 present, amplifier stages should be checked as sources of spurs. Ferrite beads are placed in amplifier stages which are *likely* to oscillate, and should therefore always be replaced after troubleshooting or repair.

9. The most likely sources of residual spurs for *field* failures will be bad bypass capacitors causing line frequency ripple on one or more of the power supply DC voltages or non-relateable spurs occurring in the Fractional-N Loop.

8-D-16. High Noise Floor. Although the 3586 is specified to have a dynamic range of 80dB, it typically is closer to 85dB. The dynamic range is established by the "phase noise" level in the First L.O. signal. Since any noise present on the A50 board can be multiplied by the ÷N number, the A50 is the most likely cause of a 3586 high-noise floor that has been isolated to the First L.O. signal. Use A50S1 to open the step loop and then use a spectrum analyzer such as the 3585A to try and locate the source of the noise. There is no easy solution to this problem so replacing likely components on A50 is the only method known.

8-D-17. Step Loop (A50) Troubleshooting.

8-D-18. Error Code E3.8. When error code E3.8 is displayed on the front panel and the red LED (A50DS70) is lit on the A50 board, it signifies that the Step Tuning Voltage has ex-

Table 8-D-3. Spurious Signal Possible Sources.

Frequencies*	Origin(s)	Using P.C. Boards
1Hz	A22	A22, A60
48-66Hz	Line Frequency	A99 (Rectifier Circuits)
80Hz	A4	A4
100(±10)Hz	A98	A98
1010(±50)Hz	A70	A70
1900(±200)Hz	A60	A60, A98
0-3400Hz	A22 (Audio)	A21, A70, A98
13.775KHz	A22 (3100Hz) LSB	A21
14.125KHz	A22 (2000Hz) LSB	A21
14.275KHz	A22 (1740Hz) LSB	A21
15.625KHz	A11	A11
15.625KHz	A10	A10, A20, A21, A22
16.425KHz	A22 (CAL-3586A)	A21
16.625KHz	A22 (CAL-3586B)	A21
16.975KHz	A22 (1740Hz) USB	A21
17.125KHz	A22 (2000Hz) USB	A21
17.475KHz	A22 (3100Hz) USB	A21
20-50KHz	A4	A4
41(±1)KHz	A61	A61
100KHz	A30, A40	A32
200-333KHz	A61	A61
500KHz	A22	A22
1MHz	A40	A11, A15, A22
1.3775MHz	A22 (3100Hz)	A22
1.4125MHz	A22 (2000Hz)	A22
1.4275MHz	A22 (1740Hz)	A22
1.6425MHz	A70 (CAL-3586A)	A22
1.6625MHz	A70 (CAL-3586B)	A22
1.6975MHz	A22 (1740Hz)	A22
1.7125MHz	A22 (2000Hz)	A22
1.7475MHz	A22 (3100Hz)	A22
2MHz	A40	A40 (Test)
2MHz	A50	A50
2-4MHz	A31, A52	A53
2-4MHz	A30	A30, A32
3-5MHz	A61	A61
3.5(±.3)MHz	A60	A60
10MHz	A16	A40
10MHz	A40	A50
10-20MHz	A30	A30
20-40MHz	A31	A30
0-32.5MHz	A15	A4, A2, A5
49.984375MHz	A11	A10
50MHz	A5	A10
50MHz	A40	A11, A15
50-82.5MHz	A51	A5, A15, A52
54-86MHz	A50	A50, A52

*No external source frequencies applied to the 3586 input.

ceeded +9V or −9V. *The loop may still be locked.* The normal range of the step loop (54-86MHz) typically produces a tuning voltage of +7.45V at 54MHz and about −3V at 86MHz. However, the high frequency end may vary from −3V by several volts since it is a function of the characteristics of the matched set of tuning diodes (A50CR1, A50CR2, A51CR1, A51CR2) which are VARICAPS. The low end (54MHz) is adjusted to 54MHz (±.1MHz) with S1 in TEST at +7.45V using A50L5, and the high end is allowed to fall where it may, voltage-wise. However, if the loop is locked at 86MHz and the STEP TUNING VOLTAGE is less than −9V, the VARICAPS (A50CR1 or A50CR2) may be bad. Be sure to replace all four VARICAPS of the matched set if any one is bad!

8-D-19. Breaking the Step Loop. There are several ways to break the step loop for troubleshooting and to test separate stages independently. Use the following procedure.

1. Remove the power from the 3586, place A50 on an extender and put A50S1 in TEST. Connect the red coax from A40J1 to A50J2. Then connect a frequency counter to the "EXT REF INPUT" BNC on the rear panel.

2. Reapply power. The counter should read 54MHz ± .1MHz. If it does not, try A50J1 to eliminate Q3/Q4. If still bad, there is a problem in the VCO or in buffer Q7/Q8. There is no simple way to identify a defective VCO component. Gain what information you can from schematic voltages (Figure 8-D-3) and then replace the VCO active components (transistors, diodes, etc.), one at a time, until the bad component is found.

3. If the loop locks up at 54MHz with A50S1 in NORMAL but won't lock up at some step frequency *other* then 54MHz (i.e., a tuned frequency other than ØHz - 1,999,999.9Hz), attach a DC source to TP1 with S1 in TEST. By driving TP1 with a DC voltage from +8V to −8V, you should be able to change the VCO frequency from 52MHz - 86MHz. If not, the VCO has a problem. This procedure should not be necessary after the preceeding step 2 unless the Step loop unlocks at some tuned frequencies but not others.

CAUTION

Do not let current from the DC source get too high while driving the VCO or other component damage may occur.

4. If the VCO is working, leave S1 in TEST (VCO ≈54MHz) to check the ÷ N Counters (U71 and U72) and the ÷ N code programming from A60. Connect a scope to U70(14) and verify that the 54MHz is getting to the counters. Connect the frequency counter to U74(6).

5. Use tuned frequency values from Table 8-D-4 to select a specific ÷ N number for the counters. If the code from A60 for that number (N) is correct and the counters are working, the frequency at U74(6) should be in the corresponding range shown in Table 8-D-4. The range is based on the VCO always being 54MHz (± .1MHz) divided by N. If the frequency is always correct at U74(6) for different values of N from Table 8-D-4, the counters (U71 and U72) are correct and so is the coding from A60.

6. If the frequency at U74(6) is incorrect for any ÷ N number, use Table 8-D-5 to verify the A60 input codes for that N. If the code is correct, one of the counters (U71 or U72) is probably bad.

7. If the A60 code *on A50* is incorrect, remove power and pull A60 out of the instrument. Ground pin B14 on XA50R and reapply power. Because of pull-up resistors RP73(2-6), the ÷ N code will appear to be 011111 (N=33). If U74(6) is now 1.633-1.640MHz (Table 8-D-4), the problem is most likely that A60 is not sending the correct codes. (Other codes may be tried if necessary by grounding the correct edge connector pin(s) to obtain a "0" for the selected code in Table 8-D-5). If the problem is A60, proceed to Service Group C and troubleshoot the A60 output circuits and then the A60 processor data lines.

8. If the counter still is not dividing correctly with A60 removed and a synthetic code provided as in Step 7, then U71 or U72 are bad. There is no simple way to tell which is bad since their outputs are tied together.

9. If the counters are good, the problem must be in the Phase Detector, switching amps or current sources. These can be checked, one-half at a time, by following steps 10-13.

10. Put A50S1 back in NORMAL. Short TP2 to ground (adjacent test pin). This will kill the input to the ÷ N and therefore the 2MHz (normal) output of the ÷ N. The reference 2 MHz should still be present at U74(11) and U75(12).

11. Now the following conditions should exist: The step frequency should drive very high (near 100MHz) because the STEP TUNE VOLTAGE should be at the negative rail (near −12V). The unlock red LED on A50 should be lit. The POSITIVE current source (Q72) should be triggering on and off in sync with the reference 2MHz. The NEGATIVE current source should be full on (Q71 on). U74(2,14) should be LOW (+3.4V) and U74(3,15) should be HIGH (+4.2V). Q75/Q76 should be turning on/off at a 2MHz rate, Q74 should be off and Q73 should be on.

12. Remove the short from TP2. Disconnect the gray cable from A40J4 to A50J3 to kill the reference 2MHz into U74/U75. The ÷ N 2MHz should again be present at U74(6).

13. Now the following conditions should exist: The step frequency should drive very low (near 45MHz) with the STEP tuning voltage above +9V. The unlock LED on A50 should be lit. The POSITIVE current source should be full on and the NEGATIVE source should be full off. U74(2,14) should be HIGH and U74(3,15) should be LOW. Q72, Q74 and Q75 should be on. Q71, Q73 and Q76 should be off.

Table 8-D-4. Troubleshooting Values for Step ÷ N.

Front Panel Tuned Frequency	÷ N Number	Frequency Range Allowable at U74(6)*
1MHz	27	1.996 - 2.004MHz
3MHz	28	1.925 - 1.933MHz
5MHz	29	1.858 - 1.866MHz
7MHz	30	1.796 - 1.804MHz
9MHz	31	1.738 - 1.746MHz
11MHz	32	1.684 - 1.691MHz
13MHz	33	1.633 - 1.640MHz
15MHz	34	1.585 - 1.592MHz
17MHz	35	1.540 - 1.546MHz
19MHz	36	1.497 - 1.503MHz
21MHz	37	1.456 - 1.463MHz
23MHz	38	1.418 - 1.424MHz
25MHz	39	1.382 - 1.388MHz
27MHz	40	1.347 - 1.353MHz
29MHz	41	1.314 - 1.320MHz
31MHz	42	1.283 - 1.289MHz
32MHz	43	1.253 - 1.259MHz

Notes: 1. *Assumes Step VCO is within its allowable adjustment range of 53.9MHz - 54.1MHz (paragraph 5-6.a) with A50S1 in TEST.

2. Refer to paragraph 8-D-19 for more information.

8-D-20. It should be noted that it is possible for the Step Loop to normally be locked up at 52MHz in certain single sideband (SSB) measurement modes. For example, if the tuned frequency on a 3586B is 1003Hz or less and TONE 1004Hz is selected with ENTRY FREQUENCY set to CARRIER and the CHANNEL = ↖ (LSB), the step will be 52MHz. This occurs because the processor sees that the operator has identified the tuned frequency as a telecommunications carrier and he wants to measure the tone in the lower sideband. That tone should be located 1004Hz below the carrier (1003Hz) at (−1Hz). Although in the real world, that frequency does not exist, the instrument thinks it does and will try to tune there. As a result, the step loop will drop to 52MHz, the fractional-N loop output (divided

by 10) will go to 2,000,001Hz and the First L.O. (sum loop) frequency will be 49.999999MHz. The same conditions will hold true if CARRIER mode is selected while the ENTRY FREQUENCY is set to TONE and the CHANNEL = ↗ (USB).

Table 8-D-5. Step Loop ÷N Codes.

Front Panel Tuned Frequency	F20 (11)	F10 (12)	F8 (16)	F4 (15)	F2 (14)	F1 (13)*	Step VCO Frequency #	÷ N Number
0 Hz - 1,999,999.9Hz	1	0	0	1	0	1	54MHz	27
2.0MHz - 3,999,999.9Hz	1	0	0	1	0	0	56MHz	28
4.0MHz - 5,999,999.9Hz	1	0	0	0	1	1	58MHz	29
6.0MHz - 7,999,999.9Hz	1	0	0	0	1	0	60MHz	30
8.0MHz - 9,999,999.9Hz	1	0	0	0	0	1	62MHz	31
10.0MHz - 11,999,999.9Hz	0	1	0	0	0	0	64MHz	32
12.0MHz - 13,999,999.9Hz	0	1	1	1	1	1	66MHz	33
14.0MHz - 15,999,999.9Hz	0	1	1	1	1	0	68MHz	34
16.0MHz - 17,999,999.9Hz	0	1	1	1	0	1	70MHz	35
18.0MHz - 19,999,999.9Hz	0	1	1	1	0	0	72MHz	36
20.0MHz - 21,999,999.9Hz	0	1	1	0	1	1	74MHz	37
22.0MHz - 23,999,999.9Hz	0	1	1	0	1	0	76MHz	38
24.0MHz - 25,999,999.9Hz	0	1	1	0	0	1	78MHz	39
26.0MHz - 27,999,999.9Hz	0	1	1	0	0	0	80MHz	40
28.0MHz - 29,999,999.9Hz	0	1	0	1	1	1	82MHz	41
30.0MHz - 31,999,999.9Hz	0	1	0	1	1	0	84MHz	42
32.0MHz - 32.5MHz	0	1	0	1	0	1	86MHz	43

Notes: 1.*Pin numbers (11) - (16) are on resistor pack RP74.
2. 0 = +2.6 VDC, 1 = +5.0 VDC.
3. # Under certain conditions, the Step VCO can be 52MHz (100110). See paragraph 8-D-20.

8-D-21. Sum Loop (A51/A52/A53) Troubleshooting.

8-D-22. Error Code E3.2. When error code E3.2 is displayed on the front panel and the (unlocked) red LED (A53DS1) on the A53 board is lit, it signifies that the difference between the STEP TUNING VOLTAGE and the SUM TUNING VOLTAGE has exceeded +1.8V or −.6V as seen at A53TP2. This can occur for many reasons. The step and fractional-N loop frequencies are controlled by the processor and they, in turn, determine the sum loop frequency. The operation of the A53 Loop Sync Comparator circuit is to try and keep the sum loop tuning voltage close enough to the step loop tuning voltage so that their difference (seen at TP2) is between −.6V and +1.8V. This will keep comparators U3A and U3B at rest (untripped condition). Since the sum voltage at U1(3) normally tracks the step voltage at U1(2), voltage measurements at these two pins and at TP2 should identify what is happening. The sum tuning voltage should track very closely to the step tuning voltage over the whole range of the First L.O. since the tuning diodes for both VCO's are a matched set. However, the sum VCO will be at 52MHz (±.1MHz) for +7.45V compared to the step loop's 54MHz (±.1MHz) at +7.45V.

8-D-23. If the step loop tuning voltage at A53TP5 is about +7.45V at 54MHz, and the sum tune voltage is sufficiently different to trip one of the comparators (U3A or U3B), then the problem is either in the sum loop or the fractional-N loop. To determine which, first tune the 3586 to 1.25MHz. Next check both of the 2-4MHz signals coming into the sum phase detector by putting A53 on an extender and looking at edge connector pins B12 and B14 of XA53 with a frequency counter.

8-D-24. If the frequency at XA53(B14) is correct (2.75MHz), then the fractional-N loop is operating correctly and the problem is in the sum loop. Proceed to paragraph 8-D-25. If the frequency is not correct at XA53(B14), then the fractional-N loop has a problem. Proceed to Service Group E and troubleshoot the fractional-N loop.