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FUJI IGBT MODULES APPLICATION MANUAL

Fuji Electric Device Technology Co., Ltd.

February 2004
REH984

CONTENT

Chapter 1
Structure and Features

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PREFACE

Power converters, such as variable-speed motor drives and uninterruptible power supplies for computers, were revolutionized with the introduction of bipolar power transistor modules and power MOSFETs. The demand for compact, lightweight, and efficient power converters has consequently also promoted the rapid development of these switching devices.
Bipolar transistor modules and MOSFETs however, cannot fully satisfy the demands of these power converters. For example, while bipolar power transistor modules can withstand high voltages and control large currents, their switching speed is rather slow.
Conversely, power MOSFETs switch fast, but have a low withstand voltage and current capacity.
Therefore, to satisfy these requirements, the insulated gate bipolar transistor (IGBT) was developed. The IGBT is a switching device designed to have the high-speed switching performance and gate voltage control of a power MOSFET as well as the high-voltage / large-current handling capacity of a bipolar transistor.

1 Structure and features

Fig. 1-1 compares the basic structure of an IGBT and a power MOSFET. The IGBT is characterized by a p^{+-} -layer added to the drain side of the power MOSFET structure. It is this p^{+-} -layer that enables the various IGBT features explained in this manual

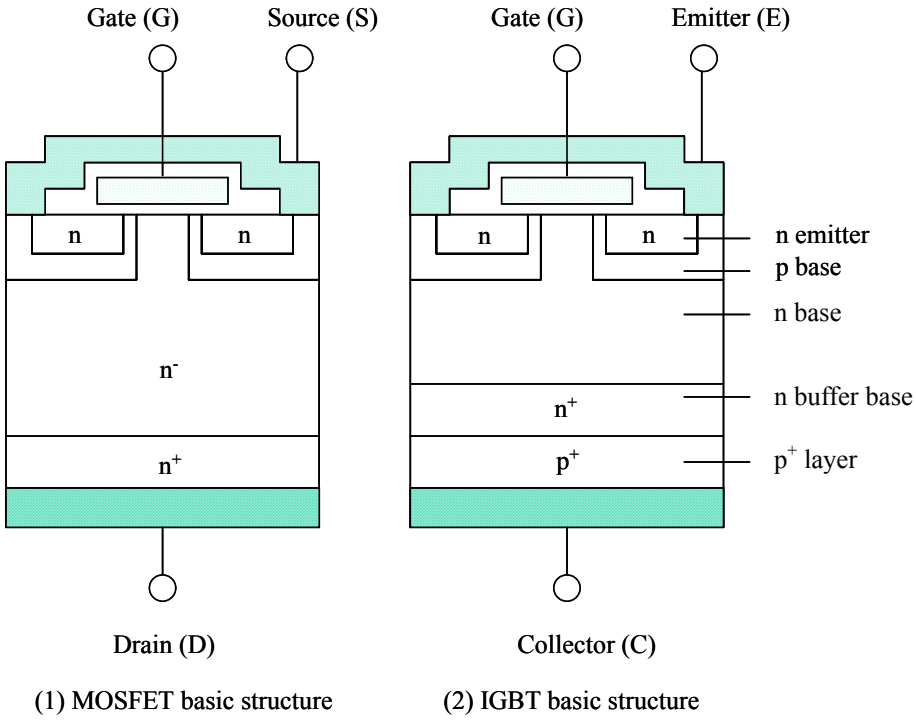


Fig. 1-1 Basic structure of MOSFET and IGBT

1.1 Voltage – controlled device

As shown in Fig. 1-2, the ideal IGBT equivalent circuit is a monolithic Bi-MOS transistor in which a pnp bipolar transistor and a power MOSFET are darlington connected. Applying a positive voltage between the gate and the emitter, switches on the MOSFET and produces a low resistance effect between the base and the collector of pnp transistor, thereby switching it on.
When the applied voltage between the gate and the emitter is set to “10”, the MOSFET will switch off, causing the supply of base current to the pnp transistor to stop and thereby switching that off as well.
This means that an IGBT can be switched on and off using voltage signals in the same way as a power MOSFET.

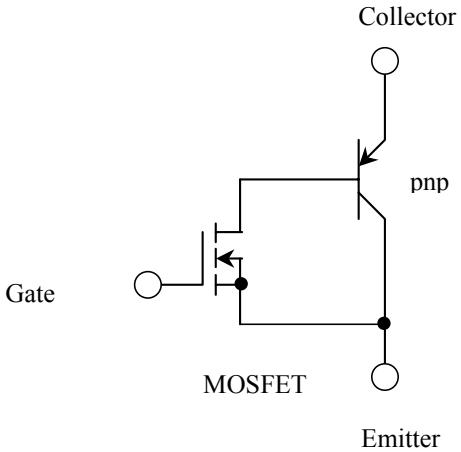


Fig. 1-2 Ideal equivalent circuit

1.2 Higher voltage and higher current switching capability than power MOSFETs

Like the power MOSFET, a positive voltage between the gate and the emitter produces a current flow through the IGBT, switching it on. When the IGBT is on, positive carriers are injected from the p^{+-}-layer on the drain side into the n-type bases layer, thereby precipitating conductivity modulation. This enables the IGBT to achieve a much lower on-resistance than a power MOSFET.

Explanation

The IGBT has a very low on resistance for the following reasons:
A power MOSFET becomes a single-layer semiconductor (n-type in the diagram) when it is in the on-state, and has resistor characteristics between the drain and the source. The higher the breakdown voltage and the device, the thicker the n-layer has to be, but this results in an increased drain-to-source resistance. Thus, as the breakdown voltage increases so does the on-resistance, making it difficult to develop large capacity power MOSFETs.
Unlike the power MOSFET, the n-base layer resistance of the IGBT becomes negligible due to the effect of the pn diode formed by the junction of the added p^{+-}-layer and n-type base layer when viewed from the drain side. As the ideal equivalent circuit in Fig. 1-2 shows, the IGBT is a monolithic cascade-type Bi-MOS transistor that consists of a pnp bipolar transistor and a power MOSFET connected in Darlington form.
The device can be compared to a hybrid cascade-type Bi-MOS transistor that consists of a bipolar transistor chip and a power MOSFET chip. The major difference is the on-resistance of the power MOSFET. The on-resistance is extremely small in the IGBT. Considering the chip for inter-chip wiring, the IGBT is superior to the hybrid cascade-type Bi-MOS transistor.

2 FUJI's IGBTs

Fuji Electric Device technology (FDT) began producing and marketing IGBTs (insulated gate bipolar transistors) in 1988 and has been supplying them to the market ever since. Fig. 1-3 is an overview of the development of, and technologies implemented in the first five IGBT generations. FDT succeeded in enhancing the characteristics of the first three IGBT generations, by using epitaxial wafers, optimizing the lifetime control techniques, and by applying fine patterning technology. The company was able to significantly enhance the characteristics of the fourth and fifth generations by switching from epitaxial wafers to FZ (floating zone) wafers. This achievement brought about a revolutionary transition in conventional approaches to IGBT design.
The basic design concept of epitaxial wafer-based IGBTs (the third and fourth generations rated at up to 600V, called "punch-through" (PT) IGBTs) is described below. These IGBTs were injected with a carrier at a high level from the collector side so that they would be filled up with the carrier to reduce the on voltage when they are turned on. In order to obtain this on voltage reduction, an n-buffer layer supporting a higher voltage was built in the FZ wafer to achieve a thinner n-layer. Moreover, a lifetime control technique was implemented to remove the carrier filling up the IGBTs so as to lessen the switching loss (Eoff) when they are turned off.

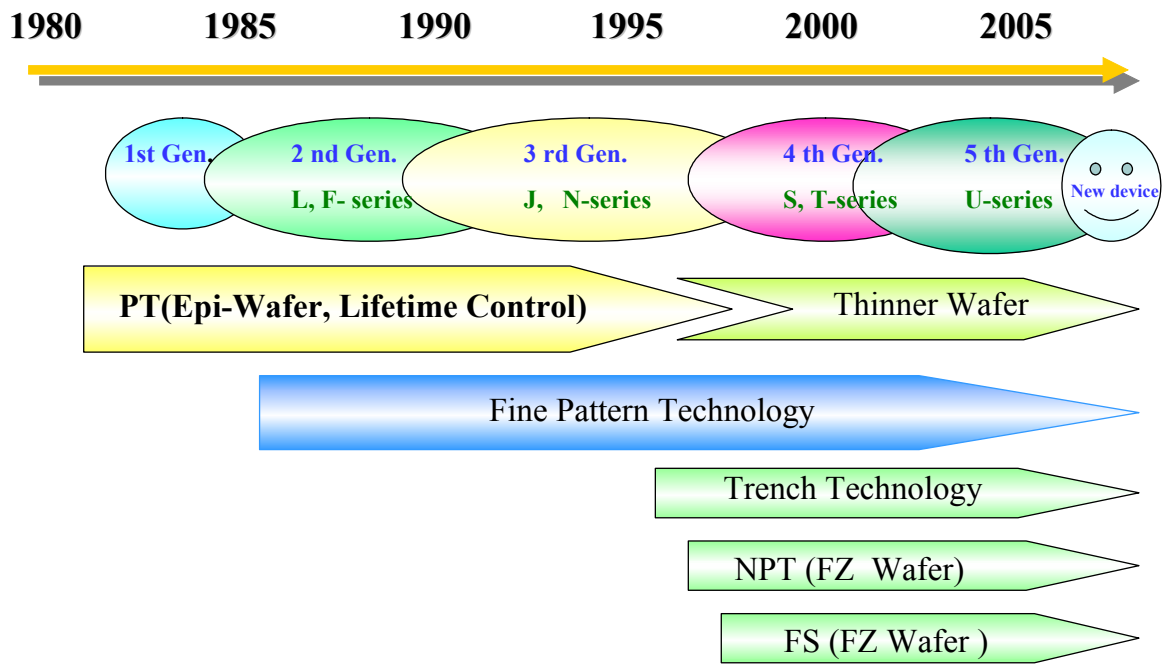


Fig. 1-3 Developments in technologies implemented in Fuji Electric IGBTs

Implementing lifetime control techniques led to increased on voltage because its effect (reduced carrier transport efficiency) persisted even in the regular on state. FDT initially worked around this problem by pursuing higher-level carrier injection. The basic design concept of epitaxial wafer-based IGBTs can be simply expressed in the wording "higher-level injection and lower transport efficiency." In contrast, FZ wafer-based IGBTs (fourth-generation 1200V IGBTs and later) implement the opposite approach to the basic design concept, such that carrier injection from the collector is suppressed to reduce injection efficiency and thus boost transport efficiency. The aforementioned design concept of higher-level injection and lower transport efficiency implemented in epitaxial wafer-based IGBTs had a limited effect in terms of characteristics enhancement as it took the illogical approach of using lifetime control techniques to suppress a carrier that had already been injected with a carrier. Moreover, the use of lifetime control resulted in certain effects that were detrimental to addressing the then growing need for the parallel use of IGBTs. One of these was increased variation in on voltage characteristics caused by lifetime control. The new FZ wafer-based non-punch through (NPT) IGBT (implemented from the fourth generation) and field stop (FS) IGBT (implemented from the fifth generation) were the result of technologies we developed to deal with these problems. The IGBTs are essentially designed to control the impurity level of the collector (p+ layer), without relying on lifetime controls, to suppress carrier injection efficiency. Yet, Fuji Electric had to work out an IGBT that withstood voltages as high as 1200V and that was as thin as one hundred and several tens of microns to achieve characteristics superior to those of an epitaxial wafer-based IGBT. (With a FZ wafer-based NPT or FS IGBT, the n-layer would approximate the chip (wafer) in thickness, and less thickness meant a lower on voltage.) In other words, the development of an FZ-wafer based IGBT has been a constant struggle for ever-thinner wafers.
FDT has launched a new line of NPT IGBTs that have evolved out of the fourth generation of 1200V IGBTs, as the S-series resolve these tasks. The company has made progress in developing 600V IGBTs requiring less thickness to such point that the market release of the 600V U series (fifth generation) is just around the corner. The U-series fifth generation of 1200V IGBTs has advanced from the NPT structure to the New FS structure to achieve enhanced characteristics that surpass the

S series. The FS structure, while adhering to the basic design concept of the lower-level carrier injection and higher transport efficiency with a lifetime control-free process, has an n-buffer layer supporting a higher voltage was built in the FZ wafer to achieve an IGBT structure that is thinner than the NPT structure. The company has completed preparations for putting on the market the resultant U-series of 1200V IGBTs which has an on voltage that is lower than that of the S-series. This technology is also implemented in a high withstand voltage line of 1700V IGBTs, which will soon be put on the market as well.

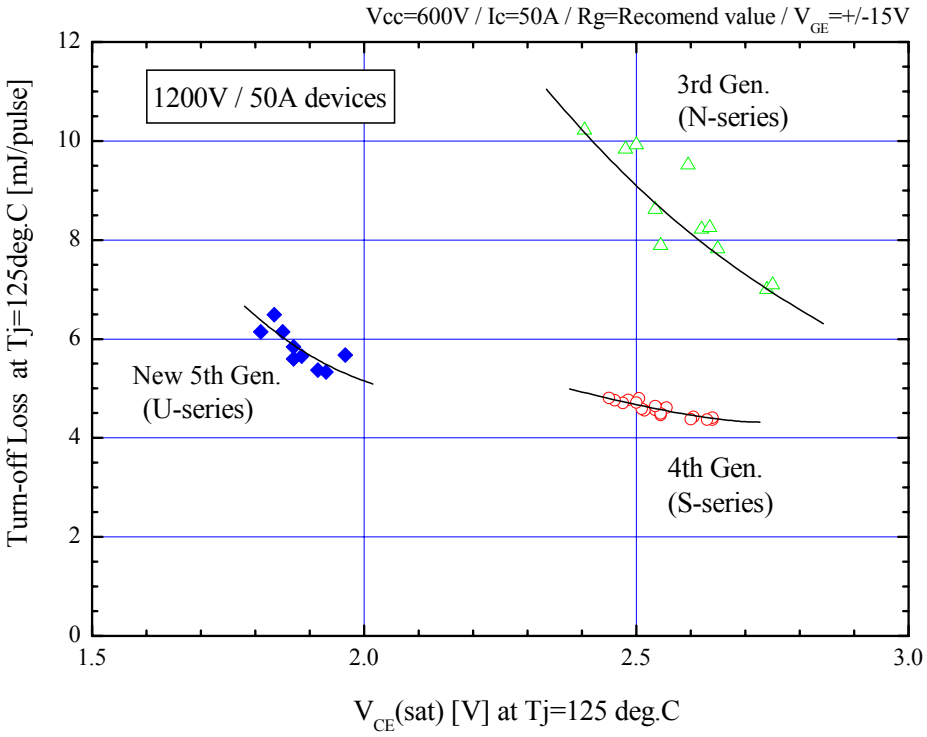


Fig. 1-4 Improved tradeoff characteristics

FDT has also pursued a finer-patterned surface structure as a technological prerequisite to enhancing IGBT characteristics. (Because an IGBT is made up of numerous IGBT blocks, fine patterning should allow a lower on voltage to be attained for more IGBT blocks.) FDT was able to realize more enhanced characteristics with the first four IGBT generations in terms of fine patterning in a planar structure (in which IGBTs are fabricated in a planar pattern). However, the company was able to dramatically enhance the characteristics with the fifth generation of the 1200V and 1700V lines of IGBTs, as a result of a technical breakthrough it made in fine pattern technology by drilling trenches in the Silicon (Si) surface. (Fig. 1-4 shows developments in the improvement of characteristics in the 1200V line.)

3 Gate controlled overcurrent protection

The most difficult challenge in producing an IGBT was making gate controlled protection possible. Differing from the ideal equivalent circuit shown in Fig. 1-2, the actual IGBT is a combination of thyristor and MOSFET as shown in Fig. 1-5.
The circuit design in Fig. 1-5 has one problem however, if the thyristor is triggered, then the IGBT cannot be turned off. This phenomenon, known as “latch-up”, may allow an overcurrent to destroy the device.
To prevent this “latch-up phenomenon”, the following techniques are used:

1) Reducing the base-emitter resistance makes the device less susceptible to latch-up.
2) Optimizing the thickness of the n^+ -buffer layer and the impurity concentration, allows the h_{FE} of the pnp transistor to be controlled.
3) Implementing a lifetime killer, allows the h_{FE} of the pnp transistor to be controlled.

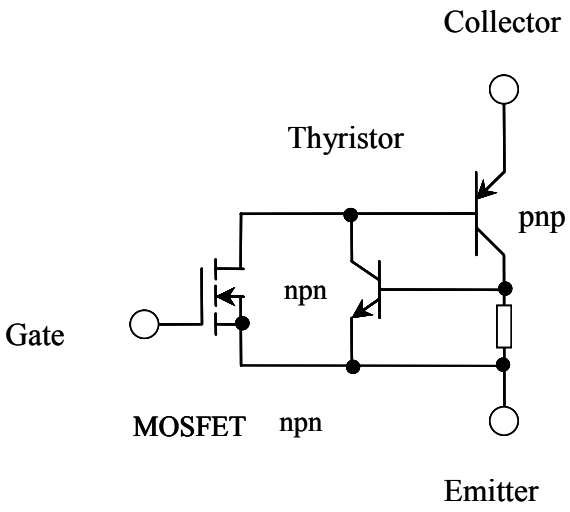


Fig. 1-5 Practical equivalent circuit

Using the above techniques, high speed, high voltage and high current IGBTs that don’t latch-up can be produced.

4 Overcurrent limiting feature

During operation, a load short-circuit or similar problem may cause an overcurrent in the IGBT. If the overcurrent is allowed to continue, the device may quickly overheat and be destroyed. The time span from the beginning of an overcurrent to the destruction of the device, is generally called the “short-circuit withstand capability time”.
The IGBT module has the ability limited to several times the devices current rating. In the event of a short circuit, the overcurrent is limited, giving the device a high short-circuit withstand capability.

5 Module structures

Fig. 1-6 and Fig. 1-7 show typical IGBT module structures. The module integrated with a terminal block shown in Fig. 1-6 has a case and external electrode terminals molded into a single unit to reduce the number of parts required and cut the internal wiring inductance. In addition, the use of a direct copper bonding (DCB) substrate makes for a high-reliability product that combines low thermal resistance and high transverse breaking strength.

The wire terminal connection structure module shown in Fig. 1-7 has main terminals bonded to the DCB substrate by wire, rather than by soldering, to simplify and downsize the package structure. This results in cuts in both thickness and weight, and fewer assembly person-hours.

Other design considerations implemented include an optimal IGBT and FWD chip layout to assure efficient heat distribution and the equal arrangement of IGBT devices in the upper and lower arms to equalize turn-on transient current balances and thus prevent increases in turn-on loss.

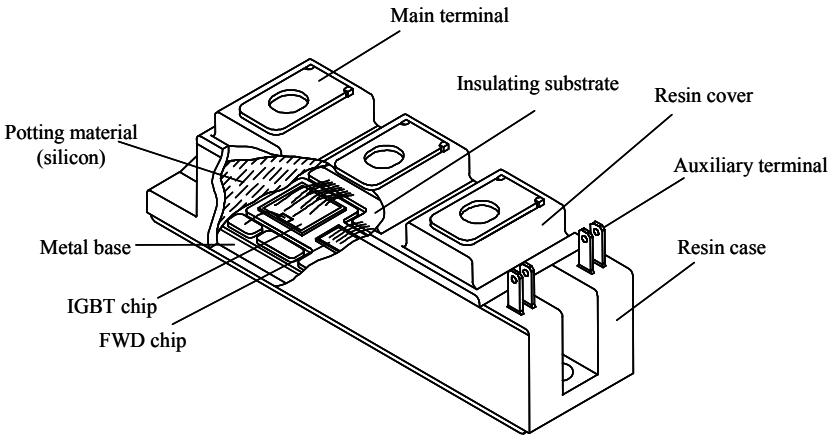


Fig. 1-6 Integrated with a terminal block type IGBT module

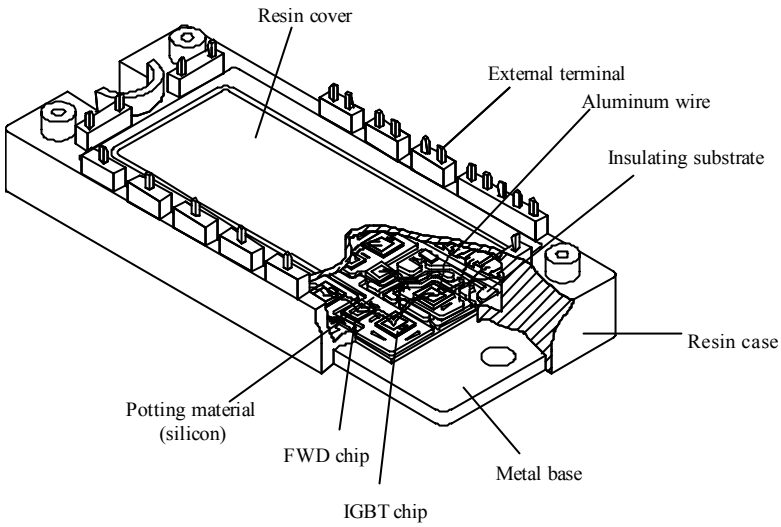
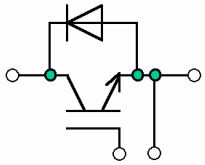
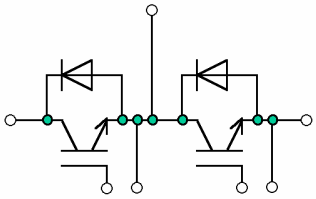
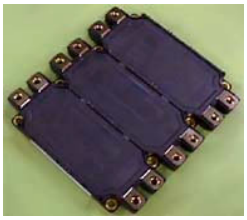
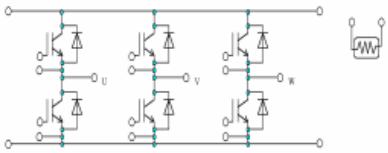
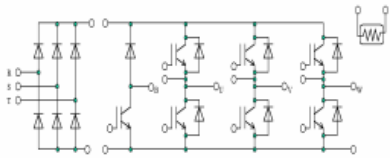


Fig. 1-7 Wire terminal connection structure type IGBT module

6 Circuit configuration of IGBT module

Table 1-1 shows typical circuit configuration of IGBT modules.
IGBT modules are configurationally grouped into four types: 1 in 1, 2 in 1, 6 in 1, and PIM (7 in 1). A circuit configuration is prescribed for each of these types. A summary description of the features of each type is also included in the figure to aid you in your device selection.

Table 1-1 Circuit configuration of IGBT modules

Type	Example of IGBT module		Features
	External view	Equivalent circuit	
1 in 1	 Example: 1MBI600S-120		Each product contains one IGBT chip and one FWD chip. Products having a high current rating are often connected in parallel in large capacity applications.
2 in 1	 Example: 2MBI450UE-120		Each product contains two IGBT chips and two FWD chips. Three units are generally used in a set to make up a PWM inverter. Otherwise, products having a high current rating are often connected in parallel.
6 in 1	 Example: 6MBI450U-120		Each product contains six IGBT chips and six FWD chips. Some variations contain a NTC. One unit is generally used alone to make up a PWM inverter.
PIM (7 in 1)	 Example: 7MBR75UB120		7 in1 contains seven IGBT chips and seven FWD chips in the inverter and brake section. PIM includes a converter section in addition to 7 in1. Some variations contain a NTC or a thyristor used for a electrolytic capacitor charging circuit.

Chapter 2
Technical Terms and Characteristics

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This section explains relevant technical terms and characteristics of IGBT modules.

1 IGBT terms

Table 2-1 Absolute maximum ratings

Term	Symbol	Definition explanation (See specifications for test conditions)
Collector-emitter voltage	V_{CES}	Maximum collector-emitter voltage with gate-emitter shorted
Gate-emitter voltage	V_{GES}	Maximum gate-emitter voltage with collector-emitter shorted
Collector current	Ic	Maximum DC collector current
	Ic pulse	Maximum pulse collector current
	-Ic	Maximum forward DC current of internal diode
	-Ic pulse	Maximum forward pulse current of internal diode
Maximum power dissipation	Pc	Maximum power dissipation per element
Junction temperature	Tj	Chip temperature during continuous operation
Storage temperature	T_{stg}	Temperature range for storage or transportation, when there is no electrical load on the terminals
FWD I^2t	I^2t	Value of joule energy (value of integration of overcurrent) that can be allowed within the range which device does not destroy. The overcurrent is defined by a line frequency sine half wave (50, 60Hz) and one cycle.
FWD surge current	I_{FSM}	The maximum value of overcurrent that can be allowed in which the device is not destroyed. The overcurrent is defined by a line frequency sine half wave (50, 60Hz).
Isolation voltage	V_{iso}	Maximum effective value of the sine-wave voltage between the terminals and the heat sink, when all terminals are shorted simultaneously
Screw torque	Mounting	Maximum and recommended torque when mounting an IGBT on a heat sink with the specified screws
	Terminal	Maximum and recommended torque when connecting externals wires to the terminals with the specified screws

Caution: The absolute maximum ratings must not be exceeded under any circumstances.

Table 2-2 Electrical characteristics

Term		Symbol	Definition explanation (See specifications for test conditions)
Static characteristics	Zero gate voltage collector current	I_{CES}	Collector current when a specific voltage is applied between the collector and emitter with the gate and emitter shorted
	Gate-emitter leakage current	I_{GES}	Gate current when a specific voltage is applied between the gate and emitter with the collector and emitter shorted
	Gate-emitter threshold voltage	$V_{GE(th)}$	Gate-emitter voltage at a specified collector current and collector-emitter voltage
	Collector-emitter saturation voltage	$V_{CE(sat)}$	Collector-emitter voltage at a specified collector current and gate-emitter voltage
	Input capacitance	C_{ies}	Gate-emitter capacitance, when a specified voltage is applied between the gate and emitter as well as between the collector and emitter, with the collector and emitter shorted in AC
	Output capacitance	C_{oes}	Gate-emitter capacitance, when a specified voltage is applied between the gate and emitter as well as between the collector and emitter, with the gate and emitter shorted in AC
	Reverse transfer capacitance	C_{res}	Collector-gate capacitance, when a specified voltage is applied between the gate and emitter, while the emitter is grounded
	Diode forward on voltage	V_F	Forward voltage when the specified forward current is applied to the internal diode
Dynamic characteristics	Turn-on time	t_{on}	The time between when the gate-emitter voltage rises from 0V at IGBT turn-on and when the collector-emitter voltage drops to 10% of the maximum value
	Rise time	t_r	The time between when the collector current rises to 10% of the maximum value at IGBT turn-on and when collector-emitter voltage drops to 10% of the maximum value
		$t_{r(i)}$	The time between when the collector current rises to 10% and when the collector current rises to 90% of the maximum value at IGBT turn-on
	Turn-off time	t_{off}	The time between when the gate-emitter voltage drops to 90% of the maximum value at IGBT turn-off and when the collector current drops to 10% of the maximum value
	Fall time	t_f	Time required for collector current to drop from 90% to 10% maximum value
	Reverse recovery time	t_{rr}	Time required for reverse recovery current in the internal diode to decay
	Reverse recovery current	$I_{rr}(I_{rp})$	Peak reverse current during reverse recovery
Reverse bias safe operating area		RBSOA	Current and voltage area when IGBT can be turned off under specified conditions
Gate resistance		R_G	Gate series resistance (See switching time test conditions for standard values)
Gate charge capacity		Q_g	Gate charge to turn on IGBT

Table 2-3 Thermal resistance characteristics

Term	Symbol	Definition explanation (See specifications for test conditions)
Thermal resistance	$R_{th(j-c)}$	Thermal resistance between the IGBT case and the chip or internal diode
	$R_{th(c-f)}$	Thermal resistance between the case and the heat sink, when the IGBT is mounted on a heat sink using the specified torque and thermal compound
Case temperature	T_c	IGBT case temperature

Table 2-4 Thermistor characteristics

Term	Symbol	Definition explanation (See specifications for test conditions)
Thermistor resistance	Resistance	Thermistor resistance at the specified temperature
B value	B	Temperature coefficient of the resistance

2 IGBT characteristics

This section illustrates the characteristics of the new 5th- generation IGBT modules, using the U series 6MBI100UB-120 (1200V, 100A) as an example.

2.1 Static characteristics

While the IGBT is on, the collector-emitter voltage (V_{CE}) changes in accordance with the collector current (I_C), gate voltage (V_{GE}), and temperature (T_j). The V_{CE} represents a collector-emitter voltage drop in the ON state, and is used to calculate the power dissipation loss of the IGBT. The smaller the V_{CE} value, the lower the power dissipation loss. Therefore, it is necessary to design the IGBT to have the smallest V_{CE} value possible.

The dependence of V_{CE}-V_{GE} on I_C is shown on the graph in Fig. 2-1 (T_j=25°C), and Fig. 2-2 (T_j=125°C). V_{CE} increases in direct proportion to the collector current and inversely proportional to the V_{GE} value. Note that when the Ic value is small, as T_j increases V_{CE} decreases, and when the I_C value is large, as T_j increases V_{CE} increases. Keep this in mind when determining operating conditions.

It is generally recommended to keep V_{GE} at 15V, and the collector current at the rateed I_C current or lower.

Fig. 2-3 shows the standard of V_{GE} in the limit that loss of V_{CE} increases rapidly in the graph where the data of Fig. 2-1 was replaced with the Ic dependency of the V_{CE} - V_{GE} characteristics.

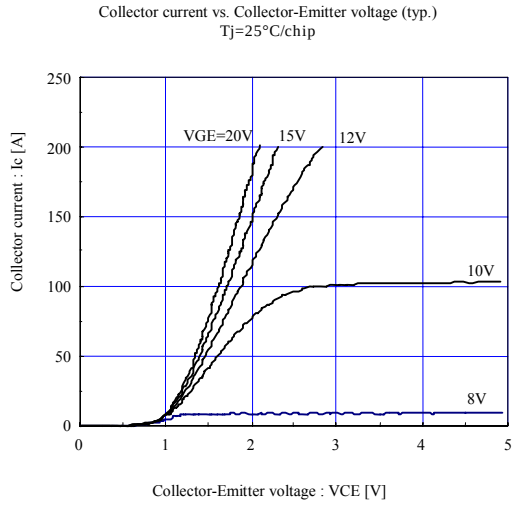


Fig. 2-1 $V_{CE(sat)}$ - I_C characteristics (Tj=25°C)

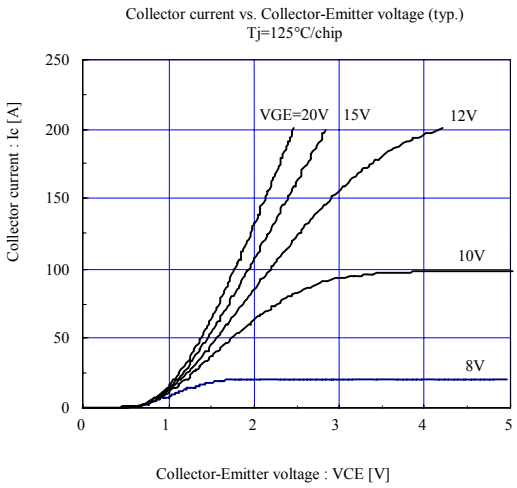


Fig. 2-2 $V_{CE(sat)}$ - I_C characteristics (Tj=125°C)

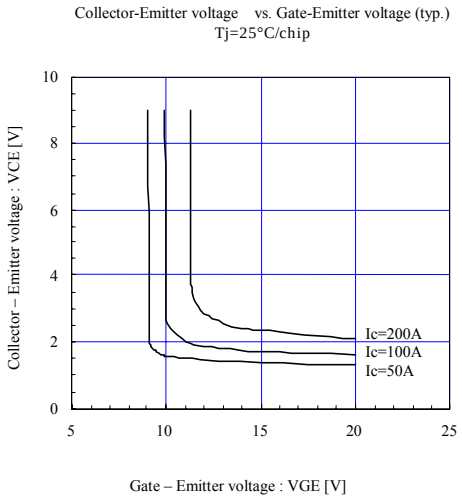


Fig. 2-3 VCE - VGE characteristics (Tj=25°C)

2.2 Switching characteristics

As the IGBT is generally used for switching, it is important to fully understand the turn-on and turn-off switching characteristics in order to determine “switching loss” (power dissipation loss at switching). It is also important to remember that these characteristics are effected by various parameters when determining operating conditions. The circuit shown in Fig. 2-4 is used to measure the four parameters of switching time, t_r, t_{on}, t_f and t_{off} as shown in Fig. 2-5. The relationship between switching time and collector current is shown in Fig. 2-5 (T_j = 25°C) and Fig. 2-6 (T_j =125°C). At greater collector currents or higher T_j, the switching time increases causing higher losses. The effect of gate resistance (R_g) vs. switching time can be seen in Fig. 2-7. When the IGBT is installed in an inverter circuit or other equipment, should the switching time (especially t_{off}) become too long, it may exceed the dead time of the upper and lower transistors, thereby causing a short-circuit. It is also important to be aware that if the switching time (t_f) is too short, the transient current change rate (di/dt) will increase and then the circuit inductance may cause a high turn-off spike voltage (L di/dt).

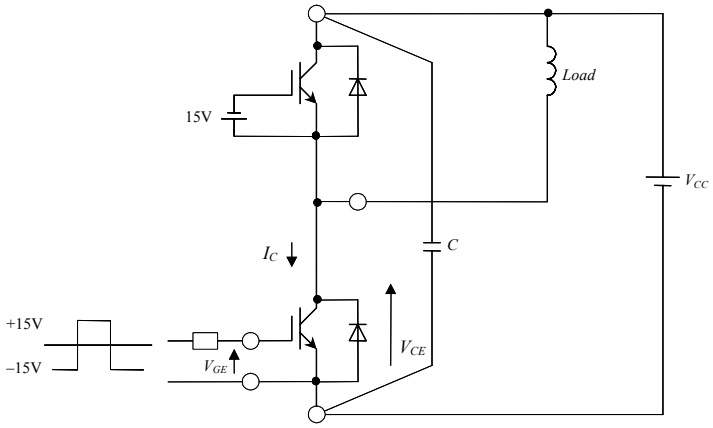


Fig. 2-4 Switching characteristics measuring circuit.

Switching loss (Eon, Eoff) occurs every time an IGBT is turned on or off, therefore it is important to minimize this loss as much as possible. As can be seen in Fig. 2-8, the greater the collector current or the higher the T_j, the greater the switching loss will be.

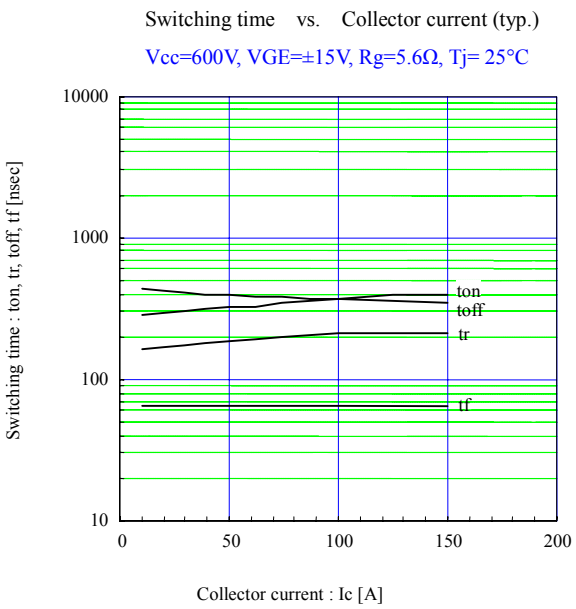


Fig. 2-5 Switching time - I_C characteristics (Tj=25°C).

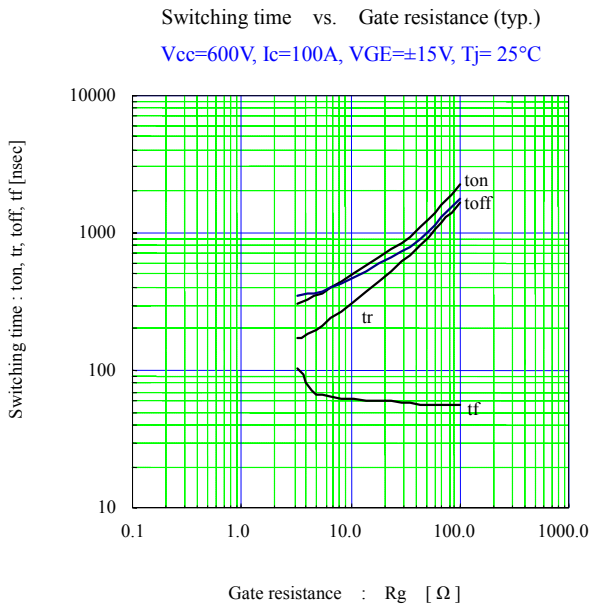


Fig. 2-7 Switching time - R_G characteristics (Tj=25°C).

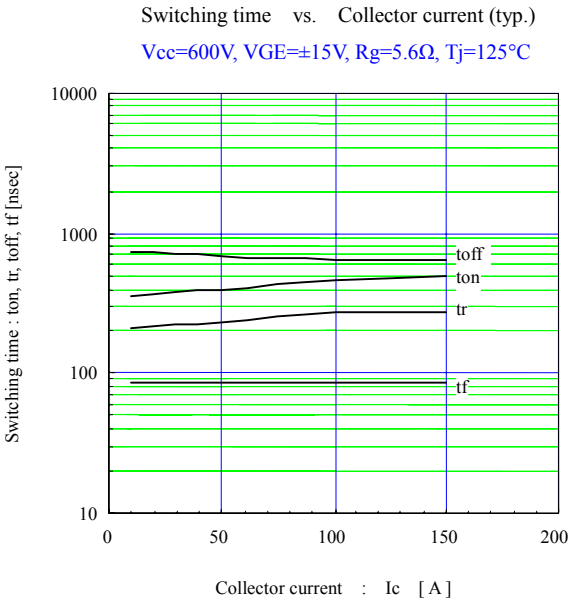


Fig. 2-6 Switching time - I_C characteristics (Tj=125°C)

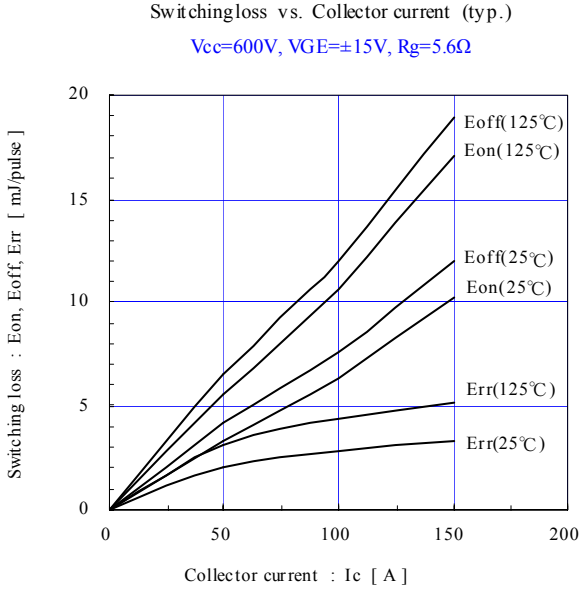


Fig. 2-8 Switching loss - I_C characteristics

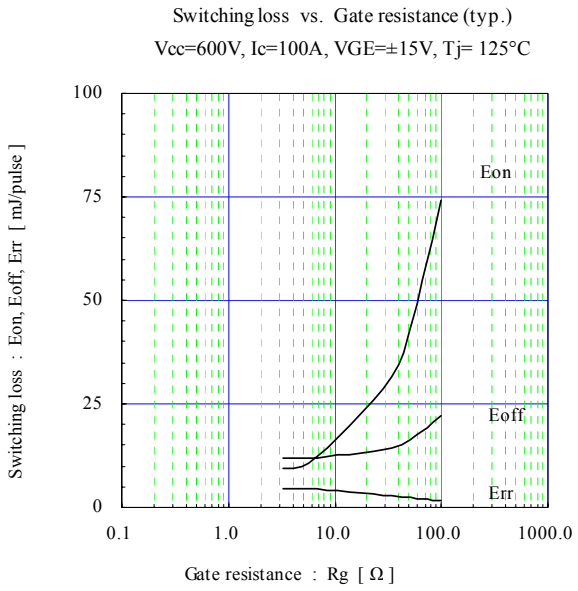


Fig. 2-9 Switching losses - R_G characteristics.

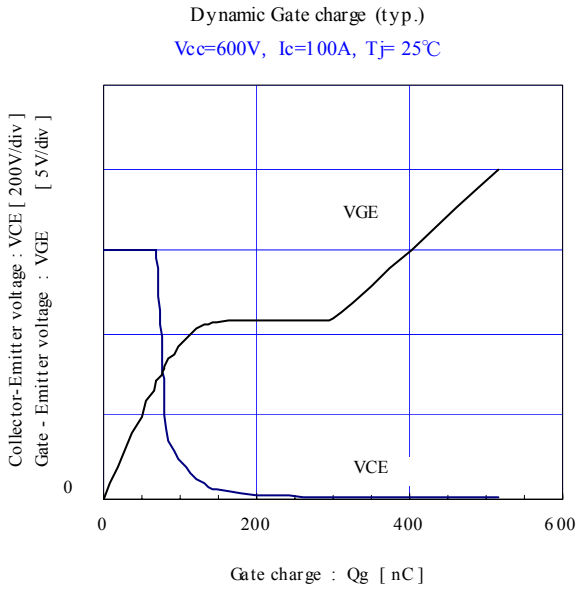


Fig. 2-10 V_{CE}, V_{GE} - Q_g characteristics

2.3 Capacitance characteristics

The gate charge capacity (Q_g) characteristics, with the main circuit supply voltage (V_{CC}) as a parameter, are shown in Fig. 2-10. Here can be seen how the collector-emitter voltage (V_{CE}) and gate-emitter voltage (V_{GE}) fluctuates when the gate charge charges. Since the gate charge capacity indicates the size of the charge required to drive an IGBT, it can be used to determine the power-supply capacity of the drive circuit.

Fig. 2-11 shows the capacitance of each of the IGBT's junctions: gate-emitter input capacitance (C_{ies}), collector-emitter output capacitance (C_{oes}) and collector-gate reverse transfer capacitance (C_{res}).

Use these characteristics along with Q_g to design your drive circuits.

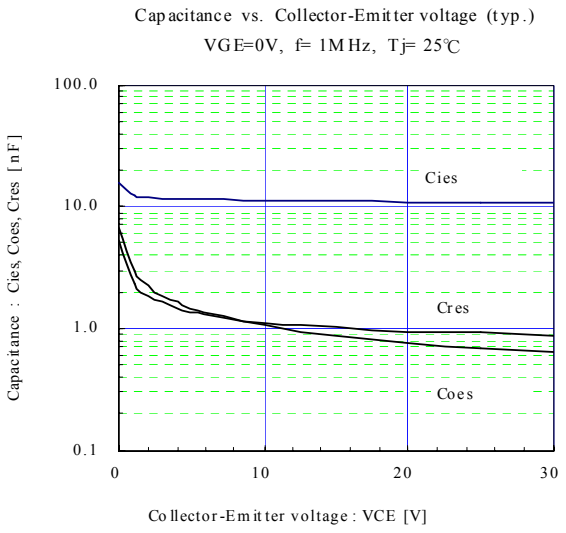


Fig. 2-11 Cies, Coes, Cres - V_{CE} characteristic

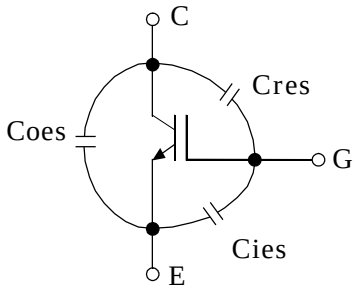


Fig. 2-12 Junction capacitance.

2.4 Safe operating areas (RBSOA and SCSOA)

When turned off, the IGBT has a safe operating area defined by V_{CE} an I_c called the “reverse bias safe operating area” or RBSOA. This area is shown by the solid line in Fig. 2-13.
It is important to design a snubber circuit that will keep V_{CC} and I_C within the limits of RBSOA when the IGBT is turned off.
Even in the case of a short-circuit (non-repetitive), an IGBT still has a safe operating area defined by V_{CE} and I_C called the “short circuit safe operating area” or SCSOA. As shown by the dotted line in Fig. 2-13, the SCSOA voltage tends to get smaller as the collector current increases.

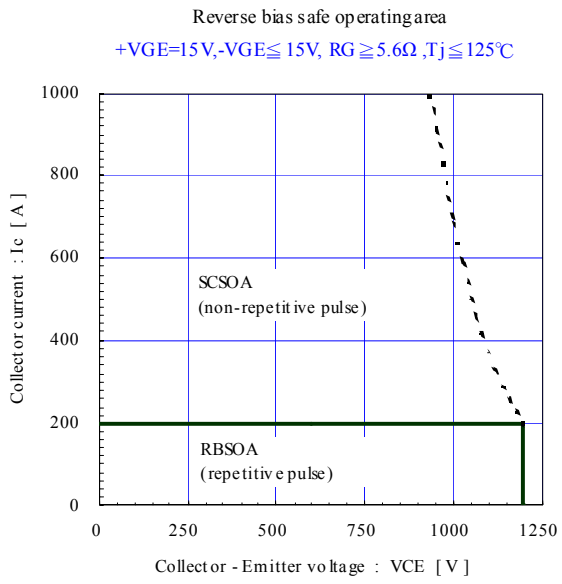


Fig. 2-13 Reverse bias safe operation area.

2.5 Internal diode (FWD) characteristics

The IGBT module has a high-speed diode (Free Wheel Diode / FWD) connected in anti-parallel with the IGBT for operating with reverse polarity. This FWD has the V_F-I_F characteristic shown in Fig. 2-14, the reverse recovery characteristic (t_{rr}, I_{rr}) shown inFig. 2-15, and the switching power loss characteristic (E_{rr}) at reverse recovery shown in Fig. 2-9. Use these characteristics to calculate the power loss in the FWD as well as the IGBT, but remember that the FWD characteristics vary in accordance with the collector current and temperature.

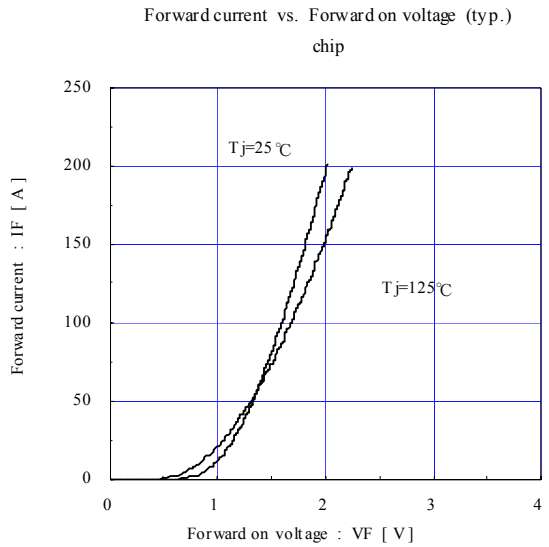


Fig. 2-14 VF - IF characteristics

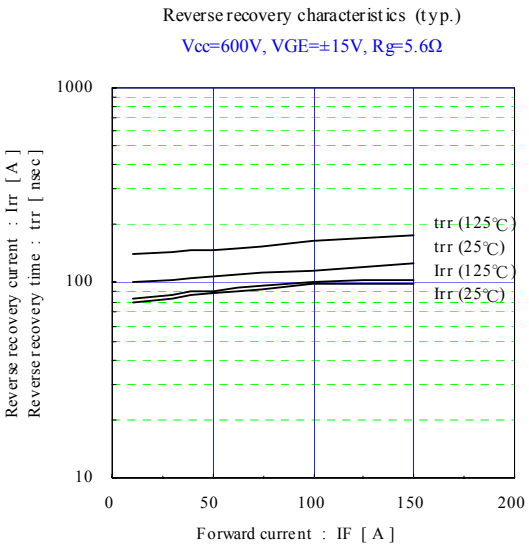


Fig. 2-15 t_{rr} , I_{rr} - I_F characteristics.

2.6 Transient thermal resistance characteristics

The transient thermal resistance characteristics, used to calculate the temperature rise of a module and to design a heat sink, are shown in Fig. 2-16.
The characteristics in the figure vary according to each individual IGBT and FWD.

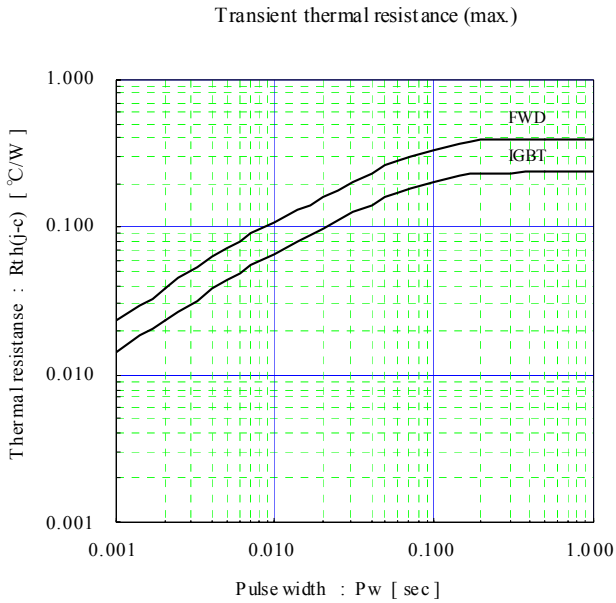


Fig. 2-16 Transient thermal resistance.

Chapter 3
IGBT Module Selection and Application

CONTENTS **Page**

This section explains relevant IGBT module selection and application.

1 Selection of IGBT module ratings

When using IGBT modules, it is important to select modules which having the voltage and current ratings most suited for the intended application.

1.1 Voltage rating

An IGBT must have a voltage rating that is suitable for dealing with the input voltage of the unit in which it will be installed. Table 1 lists IGBT voltage ratings and applicable input voltages. Use this table as a reference when selecting modules for a particular voltage application.

Table 3-1 IGBT rated voltage and applicable input voltage

	Area	IGBT rated voltage (V_{CES})			
		600V	1200V	1400V	1700V
Line voltage (Input voltage AC)	U.S.A.	208V 230V 240V 246V	460V 480V	575V	575V
	Europe	200V 220V 230V 240V	346V 350V 380V 400V 415V 440V		690V
	Japan	200V 220V	400V 440V		

1.2 Current rating

When the IGBT module's collector current increases, consequently so will the $V_{CE(sat)}$ and the power dissipation losses.
Simultaneously, there will be an increase in the switching loss, resulting in an increase in the modules temperature.
It is necessary to control the collector current in order to keep the junction temperature well below 150°C (below 125°C is recommended for safety reasons), despite the heat generated by static loss and switching loss. When designing a circuit, be careful of the fact that as the switching frequency increases, so will the switching loss and the amount of heat generated.
It is recommended to keep the collector current at or below the maximum rating for the reasons stated above. This also provides a more economical design.

2 Static electricity countermeasures

The V_{GE} of an IGBT is rated ± 20V. If an IGBT is subjected to a V_{GES} that exceeds this rated value, then there is a danger that the module might be destroyed. Therefore, ensure that the voltage between the gate and emitter is never greater than the maximum allowable value. When an IGBT is installed and voltage is applied between the collector and emitter while the gate emitter connection is open as shown in Fig. 3-1, depending on changes in the electric potential of the collector, the current (i) will flow, causing the gate's voltage to rise turning the IGBT on.
Under these circumstance, since the voltage potential between the collector and emitter is high, the IGBT could overheat and be destroyed.
On an installed IGBT, if the gate circuit is faulty or completely inoperative (while the gate is open), the IGBT may be destroyed when a voltage is applied to the main circuit. In order to prevent this destruction, it is recommended that a 10KΩ resistor (R_{GE}) be connected between the gate and the emitter.

Furthermore, since IGBT modules have a MOS structure that is easily destroyed by static electricity, observe the following points of caution.

1) When handling IGBTs, hold them by the case and do not touch the terminals.
2) If the terminals are connected by some conductive material, do not remove the material until immediately before wiring.
3) It is recommended that any handling of IGBTs be done while standing on a grounded mat.
4) Before touching a module's terminal, discharge any static electricity from your body or clothes by grounding through a high capacity resistor (1MΩ) i.e. ESD grounding strap.
   When soldering, in order to protect the module from static electricity, ground the soldering iron through a low capacity resistor.

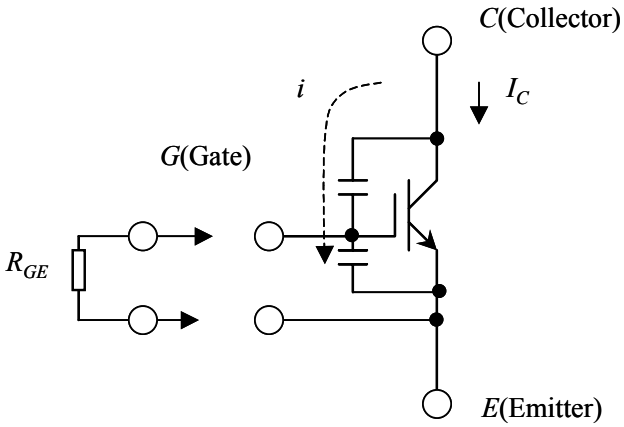


Fig. 3-1 Gate charging from electric potential of collector.

3 Designing protection circuits

Since IGBT modules may be destroyed by overcurrent, overvoltage or other abnormality, it is necessary to design protection circuits.
It is important when designing this circuits that a module's characteristics are fully taken into consideration, since an inappropriate circuit will allow the module to be destroyed. (For example, the overcurrent cut-off time may be too long or the capacitance of the snubber circuit's capacitor may be too small.)
For more details on overcurrent and overvoltage protection methods, refer to chapter 5 of this manual.

4 Designing heat sinks

As the maximum allowable junction temperature (T_j) of an IGBT module is fixed, an appropriate heat sink must be selected to keep it at or below this value.
When designing appropriate cooling, first calculate the loss of a single IGBT module, then based on that loss, select a heat sink that will keep the T_j within the required limits.
If the IGBT module is not sufficiently cooled the temperature may exceed T_j (max.) during operation and destroy the module. For more information on IGBT power loss calculation and heat sink selection methods, refer to chapter 6 of this manual.

Table 3-2 Selection of IGBT module ratings

	Motor capacity [kW]	Inverter capacity [kVA]	IGBT module type		
			N series (3rd gen.)	S series (4th gen.)	U series (5th gen.)
Input voltage 220V AC	1.5	3		7MBR30SA060	6MBI20UE-060
	2.2	4		7MBR30SA060	6MBI30UE-060
	3.7	6		7MBR50SA060	6MBI50UF-060
	5.5	9	7MBI75N-060	7MBR75SB060	6MBI75U2A-060
	7.5	13	7MBI100N-060	7MBR100SB060	6MBI100U2A-060
	11	17	2MBI150N-060		2MBI150U2A-060
	15	22			
	18.5	28	2MBI200N-060		2MBI200U2A-060
	22	33			
	30	44	2MBI300N-060	2MBI300S-060	2MBI300U2B-060
	37	55			2MBI400U2B-060
	45	67			
Input voltage 440V AC	0.75	2		7MBR10SA120	6MBI10UF-120
	1.5	3			
	2.2	4		7MBR15SA120	6MBI15UF-120
	3.7	6		7MBR25SA120	6MBI25UF-120
	5.5	9	7MBI50N-120	7MBR50SB120	6MBI50UA-120
	7.5	13			
	11	17	2MBI75N-120	6MBI75S-120	6MBI75UB-120
	15	22			
	18.5	28	2MBI100N-120	6MBI100S-120	6MBI100UB-120
	22	33			
	30	44	2MBI150N-120	2MBI150S-120	6MBI150UB-120
	37	55	2MBI200N-120	2MBI200S-120	6MBI225U-120
	45	67			
	55	84	2MBI300N-120	2MBI300S-120	6MBI300U-120

5 Designing drive circuits

It cannot be emphasized enough, that it is the design of the drive circuit that ultimately determines the performance of an IGBT. It is important that drive circuit design is also closely linked to protection circuit design.
Drive circuits consists of a forward bias voltage section to turn the IGBT on, and a reverse bias voltage section to accelerate and maintain turn-off. Remember that the characteristics of the IGBT change in accordance with the conditions of the circuit. Also, if the circuit is wired improperly, it may cause the module to malfunction. For more information on how to design the best drive circuits, refer to Chapter 7 of this manual.

6 Parallel connection

In high capacity inverters and other equipment that needs to control large currents, it may be necessary to connect IGBT modules in parallel.
When connected in parallel, it is important that the circuit design allows for an equal flow of current to each of the modules. If the current is not balanced among the IGBTs, a higher current may build up in just one device and destroy it.

The electrical characteristics of the module as well as the wiring design, change the balance of the current between parallel connected IGBTs. In order to help maintain current balance it may be necessary to match the $V_{CE(sat)}$ values of all devices.
For more detailed information on parallel connections, refer to Chapter 8 of this manual.

7 Mounting notes

When mounting IGBT modules in designated equipment, note the following:

1) When mounting an IGBT module on a heat sink, first apply a thermal compound to the module's base and then secure it properly to the heat sink by tightening the specified screws using the recommended torque. Use a heat sink with a mounting surface finished to a roughness of 10μm or less and a flatness of 100μm or less between screw mounting pitches. For more details, refer to Chapter 6 of this manual.
2) Avoid wiring designs that places too much mechanical stress on the module's electrical terminals.

8 Storage and transportation notes

8.1 Storage

1) The IGBT modules should be stored at an ambient temperature of 5 to 35°C and humidity of 45 – 75%. If the storage area is very dry, a humidifier may be required. In such a case, use only deionized water or boiled water, since the chlorine in tap water may corrode the module terminals.
2) Avoid exposure to corrosive gases and dust.
3) Rapid temperature changes may cause condensation on the module surface. Therefore, store modules in a place with minimal temperature changes.
4) During storage, it is important that nothing be placed on top of the modules, since this may cause excessive external force on the case.
5) Store modules with unprocessed terminals. Corrosion may form causing presoldered connections to have high contact resistance or potential solder problems in later processing.
6) Use only antistatic containers for storing IGBT modules in order to prevent ESD damage.

8.2 Transportation

1) Do not drop or jar modules which could otherwise cause mechanical stress.
2) When transporting several modules in the same box or container, provide sufficient ESD padding between IGBTs to protect the terminals and to keep the modules from shifting.

9 Additional points

1) If only a FWD is used and an IGBT is not used (as in a chopper circuit application), apply a reverse bias voltage of -5V or higher (-15V recommended, -20V maximum) between G and E of the IGBT out of service. An insufficient reverse bias voltage could cause the IGBT to fire falsely due to dV/dt during reverse recovery of the FWD, resulting in device destruction.

2) Measure the gate drive voltage (V_{GE}) at the terminals of the module to verify that a predetermined voltage is being applied. (Measurement at the end of the drive circuit will lead to a voltage that is unaffected by the voltage drops across the transistors and other components used at the end of the drive circuit. Consequently, if the predetermined voltage (V_{GE}) is not being applied to the IGBT gate, this lower (V_{GE}) voltage could pass unnoticed, leading to device destruction.

3) Measure the surge and other voltages appearing during turn-on and turn-off at the module terminals.

4) Avoid using the product in locations where corrosive gases are present.

5) Use the product within the tolerances of the absolute maximum ratings (voltage, current, temperature etc). Particularly, if a voltage higher than V_{CES} is applied to the module, an avalanche could occur, resulting in device destruction.

6) As a precaution against the possible accidental destruction of the device, insert a fuse or breaker of the appropriate rating between the commercial power source and the semiconductor device.

7) Before using the IGBT, acquire a full understanding of its operating environment to verify that its reliability life can be met. If the product is used past its reliability life, the device could be destroyed before the intended useful life of the equipment expires.

8) Use this IGBT within its power-cycle life capability.

9) The warranty covering the functionality, appearance and other aspects of the product will be voided if it is used in environments where acids, organic substances or corrosive gases (such as hydrogen sulfide and sulfur dioxide) are present.

10) Do not allow the primary and control terminals of the product IGBT to be deformed by stress. A deformed terminal could cause a defective contact or other fault.

11) Select the correct terminal screws for the module according to the outline drawing. Using longer screws could damage the device.

12) Do not apply excessive stress to the primary and control terminals of the product when installing it in equipment. The terminal structure could be damaged.

13) Apply sufficient reverse bias gate voltage, improper ($-V_{GE}$) could cause the IGBT to turn on when not intended. Set $-V_{GE}$ at -15V (recommended) to prevent false turn-on.

14) A high turn-on voltage (dv/dt) could cause the IGBT in the opposing arm to turn on falsely. Use the product under optimal gate drive conditions (such as $+V_{GE}$, $-V_{GE}$, and $R_{G)}$ to prevent false turn-on.

Chapter 4
Troubleshooting

CONTENTS **Page**

This section explains IGBT troubleshooting and failure analysis.

1 Troubleshooting

Incorrect wiring or mounting of an IGBT in an inverter circuit could cause module destruction. Because a module could be destroyed in many different ways, once the failure has occurred, it is important to first determine the cause of the problem, and then to take the necessary corrective action. Table 4-1, illustrates how to determine a module's failure modes as well as the original causes of the trouble by observing irregularities outside of the device. First of all, compare the device estimated failure mode to the table when an IGBT is destroyed. Fig. 4-1(a-f) was prepared as a detailed guide (analysis chart), and should be used to help investigate the destruction when you cannot determine the cause by using Table 4-1. Typical failure modes and troubleshooting are described in section 4-3 and can be used to assist in finding the cause.

Table 4-1 Causes of device failure modes

External abnormalities		Cause		Device failure mode	Further checkpoints
Short circuit	Arm short circuit	Short circuit destruction of one element		Outside SCSOA	Confirm waveform (locus) and device ruggedness match during an arm short circuit.
	Series arm short circuit	Gate or logic Circuit malfunction	Noise, etc.	Outside SCSOA	Check for circuit malfunction. Apply the above.
		dv/dt	Insufficient gate reverse bias. Gate wiring too long	Overheating	Check for accidental turn-on caused by dv/dt.
		Dead time too short	Insufficient gate reverse bias. Date time setting error	Overheating	Check that elements t_{off} and deadtime match.
	Output short circuit	Miswiring, abnormal wire contact, or load short circuit.		Outside SCSOA	Check conditions at time of failure. Check that device ruggedness and protection circuit match. Check wiring condition.
	Ground short	Miswiring, abnormal wire contact		Outside SCSOA	
Overload		Logic circuit malfunction Overcurrent protection circuit setting error		Overheating	Check logic circuit. Check that overload current and gate voltage match. If necessary, adjust overcurrent protection level.
Over Voltage	Excessive input voltage	Excessive input voltage Insufficient overvoltage protection		C-E Overvoltage	If necessary, adjust overvoltage protection level.
	Excessive spike voltage	Switching turn-off		Outside RBSOA	Check that turn-off operation (loci) and RBSOA match. If necessary, adjust overcurrent protection level.
		FWD commutation	High di/dt resulting	C-E Overvoltage	Check that spike voltage and device ruggedness match. If necessary, adjust snubber circuit.
			Transient on state(Short off pulse reverse recovery)		Check logic circuit. Gate signal interruptions resulting from noise interference.
Drive supply voltage drop		DC-Dc converter malfunction		Overheating	Check circuit.
		Drive voltage rise is too slow.		Overheating	
		Disconnected wire		Overheating	
Gate overvoltage		Static electricity Spike voltage due to excessive length of gate wiring		Avalanche Overvoltage	Check operating conditions (anti-static protection). Check gate voltage.

External abnormalities		Cause		Device failure mode	Further checkpoints
Overheating	Overheating	Loose terminal screw or cooling fan shut down		Overheating	Check cooling conditions. Check logic circuit. Logic circuit malfunction
	Thermal runaway	Logic circuit malfunction		Overheating	
Stress	Stress	The soldering part of the terminal is disconnected by the stress fatigue.	Stress from external wiring	Disconnection of circuit	Check the stress and mounting parts.
	Vibration		Vibration of mounting parts		
Reliability (Life time)		The application condition exceeds the reliability of the module.		Destruction is different in each case.	Refer to Fig. 4-1 (a-f).

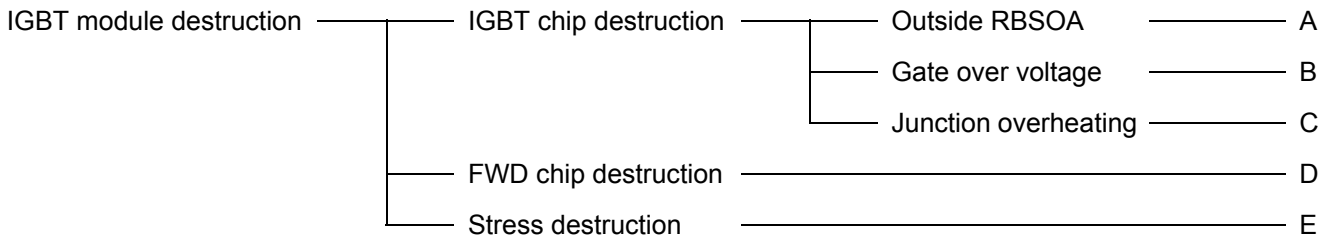


Fig. 4-1(a) IGBT module failure analysis

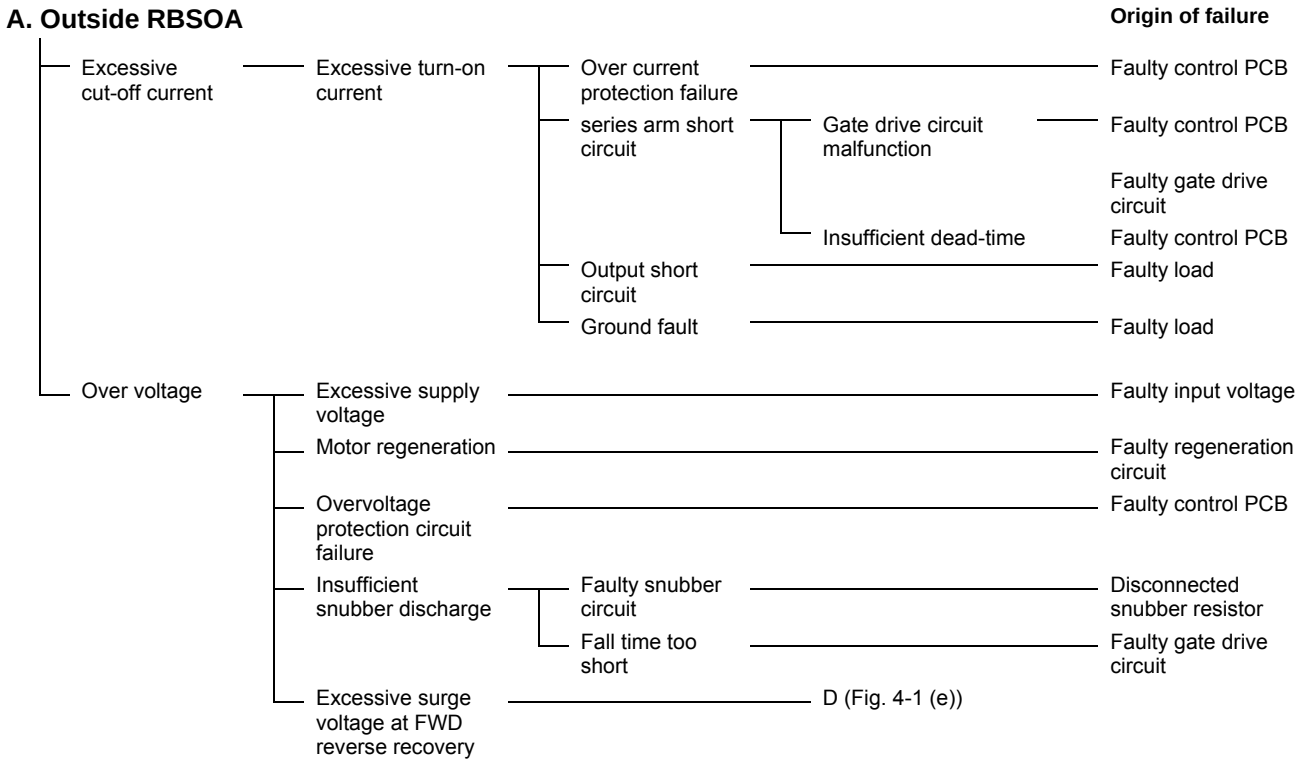


Fig. 4-1(b) Mode A: Outside RBSOA

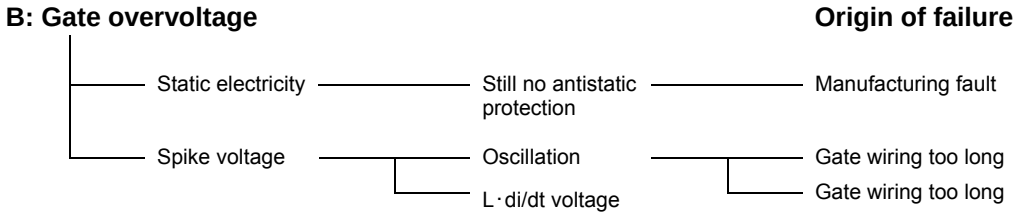


Fig. 4-1(c) Mode B: Gate overvoltage

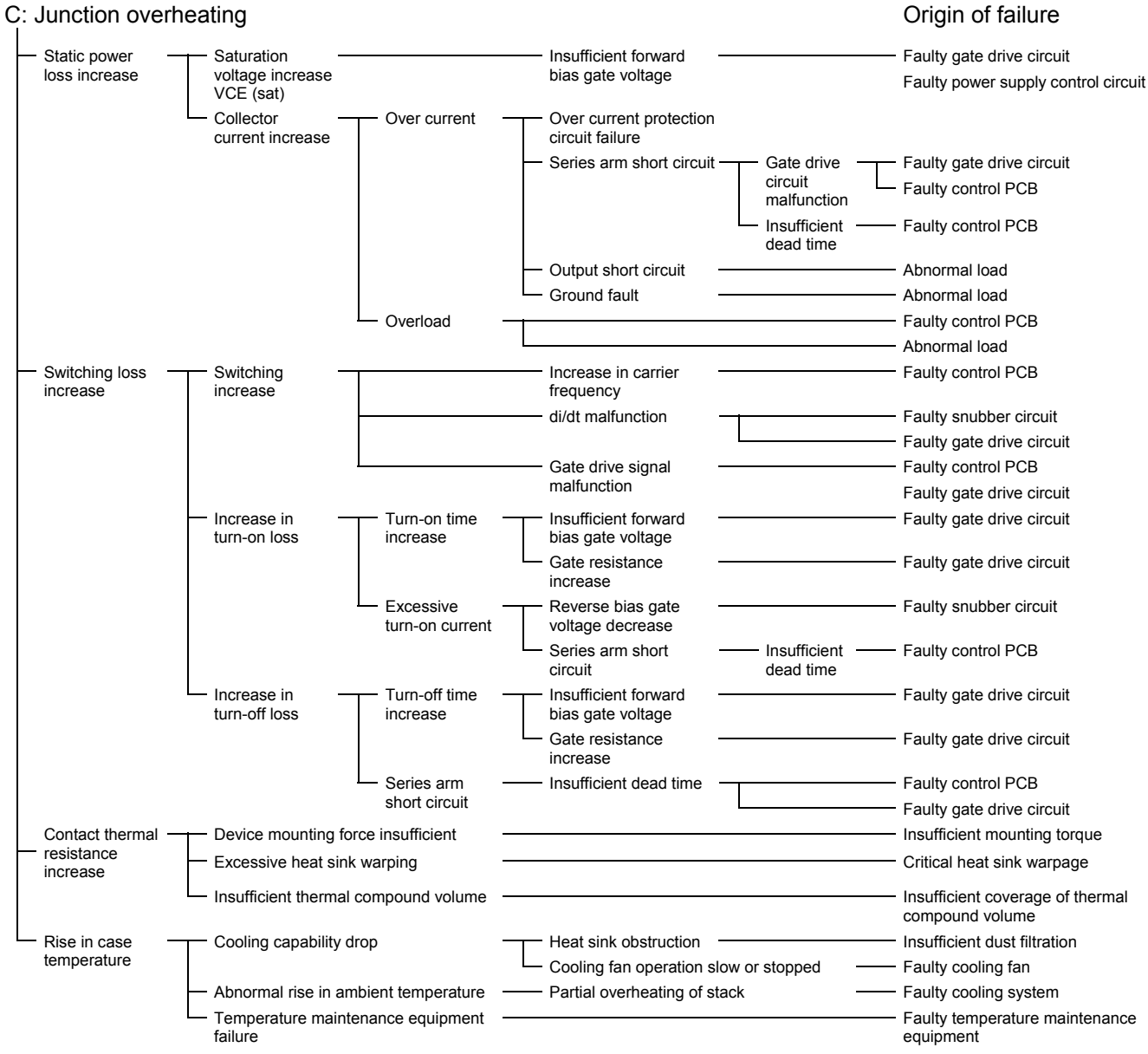


Fig. 4-1(d) Mode C: Junction overheating

D: FWD destruction

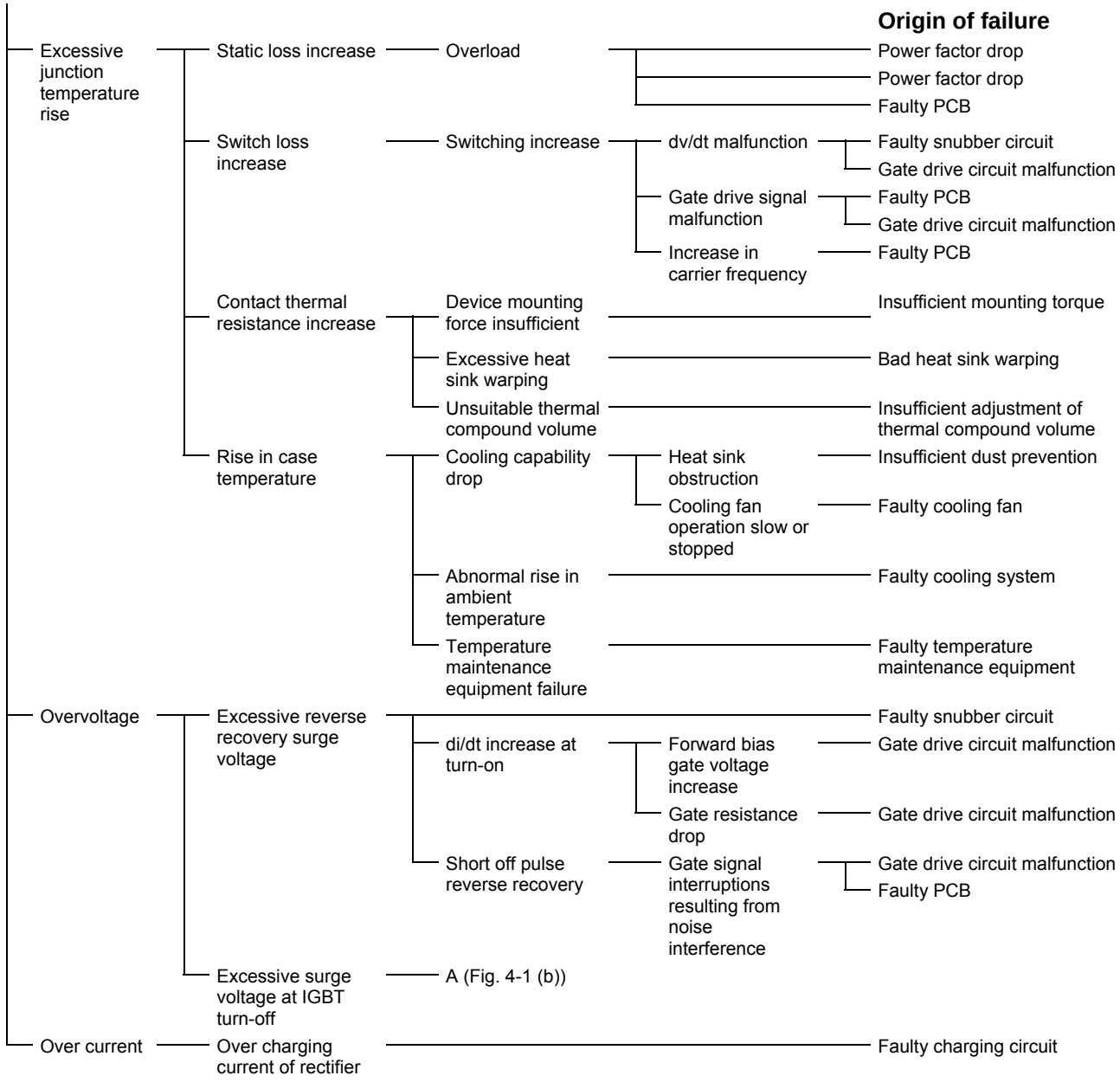


Fig. 4-1(e) Mode D: FWD destruction

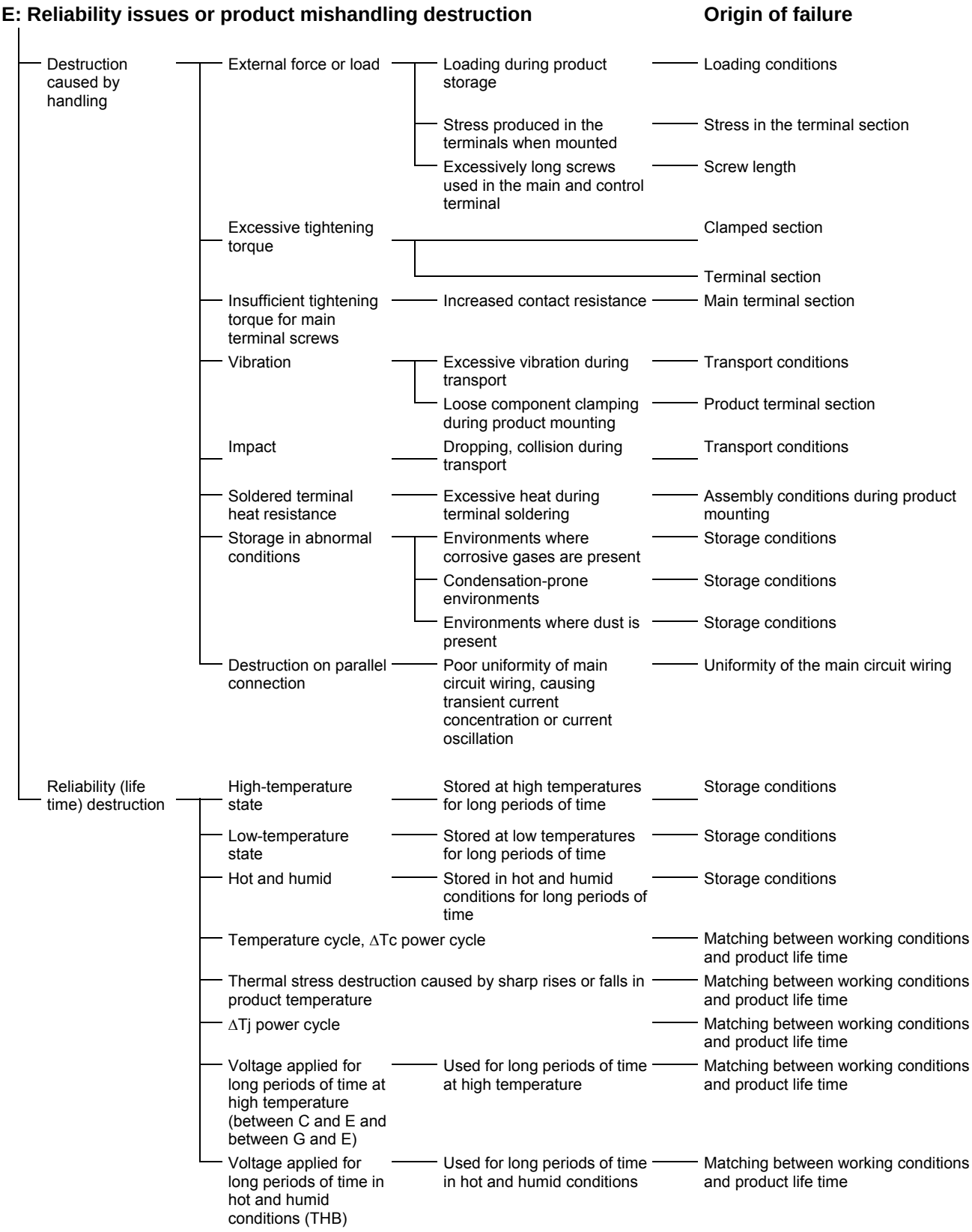


Fig. 4-1(f) Mode E: Reliability issues or mishandling destruction

2 IGBT test procedures

An IGBT module that has been found to be faulty can be checked by testing it on a transistor characteristics measuring device called a "transistor curve tracer (CT)."

(1) Leakage current between gate and emitter, and threshold voltage between gate and emitter

(2) Short circuit, breakdown voltage, open circuit between collector and emitter (Short gate and emitter.)

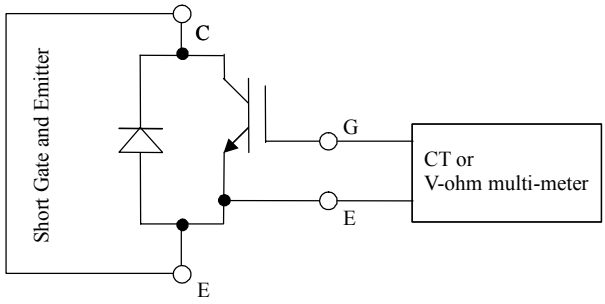


Fig. 4-2 G-E (gate) check

If a CT is not available, other test equipment, such as a Volt-ohm multi-meter that is capable of measuring voltage/resistance and so forth to determine a failure, can be used to help diagnose the destruction.

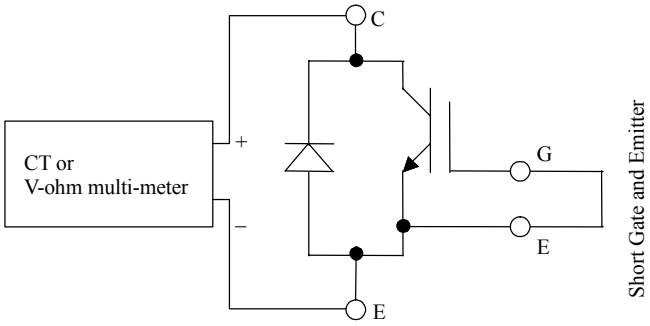


Fig. 4-3 C-E check

2.1 G-E check

As shown in Fig. 4-2, measure the leakage current or resistance between G and E, with C and E shorted to each other. (Do not apply a voltage in excess of 20V between G and E). If the V-ohm multi-meter is used, verify that the internal battery voltage is not higher than 20V.)
If the product is normal, the leakage current reading should be on the order of several hundred nano-Amps. (If the V-ohm multi-meter is used, the resistance reading would range from several tens MΩ to infinite. In other situations, the device has most likely broken down. (Generally, device destruction is represented by a short between G and E.)

2.2 C-E check

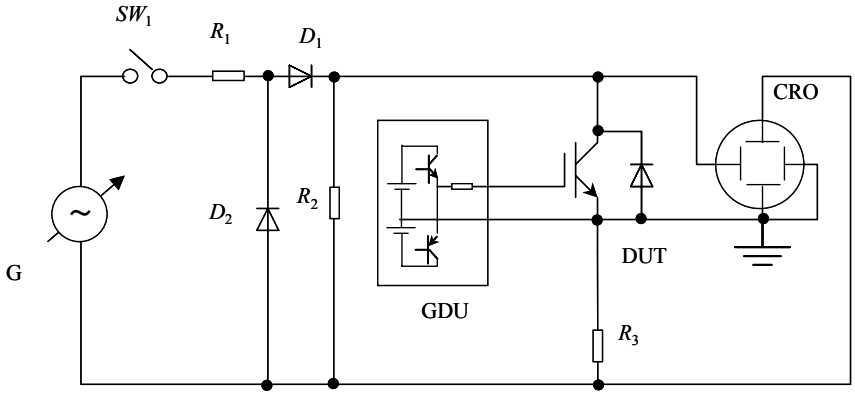
As shown in Fig. 4-3, measure the leakage current or resistance between C and E, with a short between G and E. Be sure to connect the collector to (+) and the emitter to (-). Reverse connections will energize the FWD, causing C and E to be shorted to each other.
If the module is normal, the leakage current reading should read below the I_{CES} maximum specified in the datasheet. (If the V-ohm multi-meter is used, the resistance reading would range from several ten MΩ to infinity. In other situations, the device has most likely broken down. (Generally, device destruction is represented by a short between C and E.)

Note:
Never perform withstand voltage measurement between the collector and gate. It might cause the dielectric destruction of the oxide layer in the section where a mirror capacitance is formed between the collector and gate.

3 Typical trouble and troubleshooting

3.1 Energizing a main circuit voltage when the circuit between G and E is open

If a voltage is applied to the main circuit with the circuit between the gate and emitter open, the IGBT would be turned on autonomously, triggering large current flow to cause device destruction. Be sure to drive the device with a signal placed between G and E. (This phenomenon occurs when the gate-emitter capacitance is charged through feedback capacitance Cres of the IGBT at the application of a main voltage with the circuit between G and E open, causing the IGBT to be turned on.)
If the signal line is switched using a mechanical switch, such as a rotary switch, during product acceptance testing or on similar occasions, the circuit may open instantaneously between G and E at the time of switching could cause device destruction (the phenomenon described above).
When the mechanical switch chatters, a similar period is generated, leading to device destruction. To guard against such risks, be sure to discharge the main circuit voltage (between C and E) to 0V before switching the gate signal. When performing characteristics testing, such as acceptance testing, on a product comprising multiple devices (two or more), keep the gate and emitter shorted to each other on the devices other than the one under test.
Fig. 4-4 shows an example of an on-voltage measurement circuit. The measurement sequence is described with reference to this measurement circuit. First, turn off the gate drive unit (GDU) (V_{GE} = 0V) and then turn on SW_1 to apply a voltage between C and E. Next, apply a predefined forward bias voltage between G and E from the GDU to energize the IGBT for measuring the on voltage. Lastly, turn off the gate circuit and then SW_1. Such sequencing will allow for safe measurement of device characteristics without risking destruction.

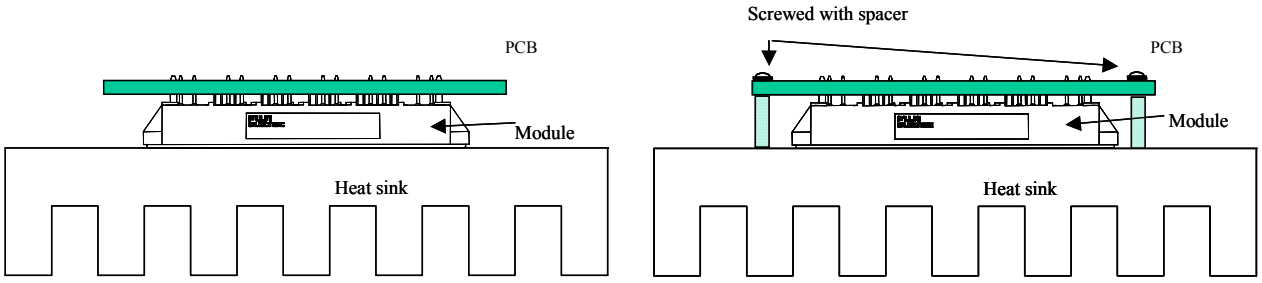


DUT : IGBT under test, GDU : Gate drive unit, G : Variable AC power supply
CRO : Oscilloscope, R_1, R_2 : Protective resistance, R_3 : Current measurement non-inductive resister
D_1, D_2 : Diode, SW_1 : Switch

Fig. 4-4 On voltage measurement circuit

3.2 Destruction caused by mechanical stress

If the terminals or pins are subjected to stress from a large external force or vibration, the internal electrical wiring of the product could be destroyed. Be careful by not mounting the device in an application that might be strenuous, minimize the chances of such destruction by reducing stress. Fig. 4-5 shows an example of mounting a gate drive printed circuit board (PCB) on top of the IGBT module.

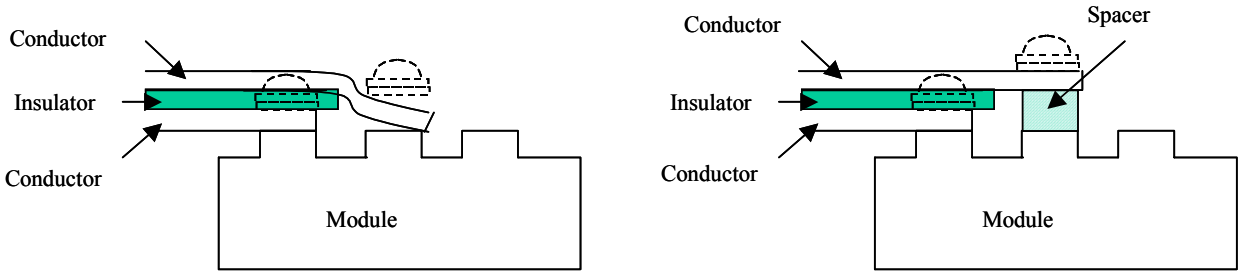


(1) Mounting that exposes module terminal to stress

(2) Mounting that exposes module terminal to stress-free (Recommended)

Fig. 4-5 Clamping a PCB

As shown in (1), if the gate drive printed circuit board is mounted without clamping the PCB, the any PCB vibration could cause flexing possibly, stressing the module pins causing pin damage or internal electrical wiring damage. As shown in (2), the PCB needs to be clamped to prevent this problem. When taking this corrective action, use a dedicated fixing material having sufficient strength.



(1) Wiring that exposes terminals to stress

(2) Wring with spacer (Recommended)

Fig. 4-6 Mounting in laminated bus bar is used

Fig. 4-6 shows an example of main circuit wiring using a laminated bus bar. If there is a step difference between the (+) and (-) electrical wiring conductors as shown in (1), the terminals are continually exposed to upward tensile stress, causing a disconnect of the internal electrical wiring. To prevent this problem, it is necessary to insert a conductive spacer to eliminate the step difference between the conductors on the parallel plate. Furthermore, a gap in the wiring height location could also generate large tensile stress or external force to the terminals in the PCB structure.

3.3 Accidental turn-on of the IGBT caused by insufficient reverse bias gate voltage $-V_{GE}$

Insufficient reverse bias gate voltage $-V_{GE}$ could cause both IGBTs in the upper and lower arms to be turned on after accidental turn-on, resulting in a short-circuit current flowing between them. A surge voltage or loss arising when this current is turned off may result in product destruction. In designing a circuit, make sure that no short-circuit currents are generated as a result of a short circuit between the upper and lower arms (recommended $-V_{GE}$ = 15V).

The occurrence of this phenomenon is described below with reference to Figs. 4-7 and 4-8.

An IGBT with $-V_{GE}$ applied is shown in Fig. 4-7. Assume that an IGBT is connected in series on the opposing arm as well, though it is not depicted. When the IGBT on the opposing arm is turned on, the FWD shown in Fig. 4-7 recovers in reverse direction. As shown in Fig. 4-8, dv/dt is generated between C and E at this time. This dv/dt causes current i_{CG} to flow through feedback resistance Cres between C and G and through gate resistance R_G as shown in Fig. 4-7. This i_{CG} induces a potential

difference of $\Delta V = R_G \times i_{CG}$ across the R_G, pushing up the V_{GE} towards the + side as shown in Fig. 4-8. If the peak voltage of V_{GE} exceeds V_{GE} (th), the IGBT is turned on, introducing short-circuit current flow through the upper and lower arms. Conversely, no short-circuit current will flow through the upper and lower arms unless the peak voltage of V_{GE} exceeds V_{GE} (th). This problem can be suppressed by applying a sufficient reverse bias voltage ($-V_{GE}$). Because the required value of V_{GE} depends on the drive circuit used, gate wiring, R_G and the like, check for the presence or absence of a short-circuit current flow through the upper and lower arms when designing a circuit.

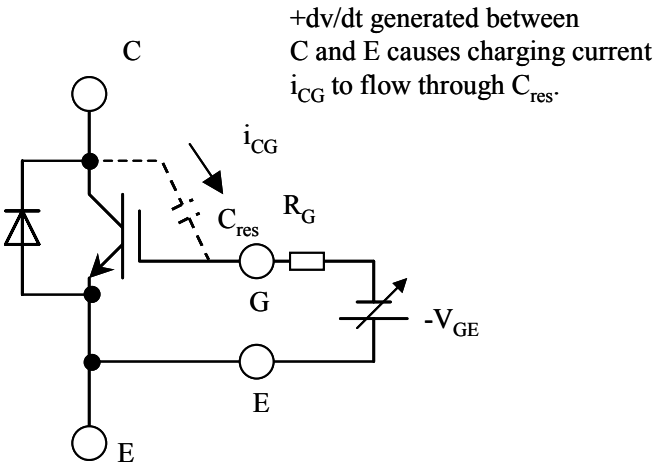


Fig. 4-7 Principles of dv/dt malfunctioning

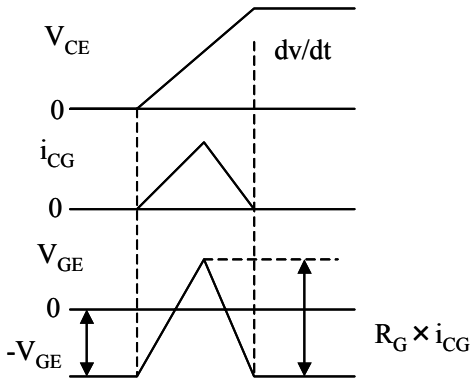


Fig. 4-8 Waveforms during reverse recovery

Fig 4-9 shows an example of the method of checking for the presence or absence of the short-circuit current flow through the upper and lower arms. First, open the inverter output terminals (U, V, W) (that is, leave them under no load) as shown. Next, activate the inverter to drive the individual IGBTs. The presence or absence of the short-circuit current flow through the upper and lower arms can be determined by detecting current flow from the power line as shown. If a sufficient reverse bias current is applied, a very weak pulse current (about 5% of the rated current) that charges the device junction capacitance will be detected. With insufficient reverse bias voltage $-V_{GE,}$ this current increases. To ensure correct determination, we recommend first detecting this current with the applied voltage $-V_{GE}$ = -15V. This eliminates the risk of false firings. Then measure the same current with the predefined value of $-V_{GE}$. If the two measurements of the current are equal, no false turn-on has occurred. A recommended solution is to increase the reverse bias voltage $-V_{GE}$ until the short-circuit current is eliminated or inserting a capacitance (C_{GE}) about half the Cies value between G and E. (Verify the applicability of the method of the C_{GE} insertion beforehand, because it will significantly affect the switching time and switching losses.)

The short-circuit current flow through the upper and lower arms is caused by insufficient dead time, as well as accidental turn-on during dv/dt described above. A short-circuit current can be observed by running the test shown in Fig. 4-9 while this phenomenon is present. If increasing the reverse bias voltage-V_{GE} does not help reduce the short-circuit current, take relevant action, such as increasing the dead time. (More detailed instructions can be found in Chapter 7.)

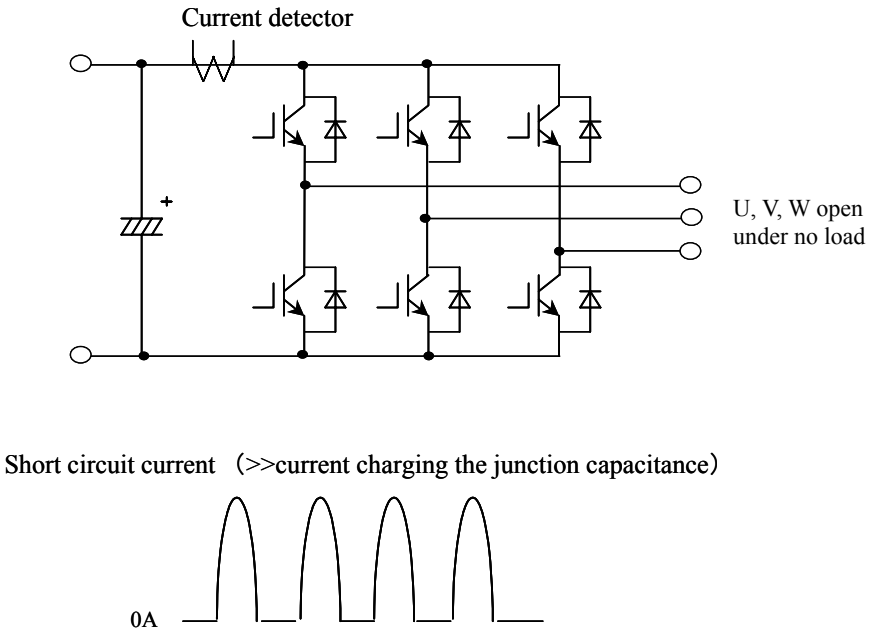


Fig. 4-9 Short-circuit current measuring circuit

3.4 Diode reverse recovery from a transient on state (Short off pulse reverse recovery)

The IGBT module contains a FWD. Paying full attention to the behavior of the FWD is very important for designing a dependable circuit. This section focuses on the less known phenomenon of short off pulse reverse recovery that could lead to product destruction.

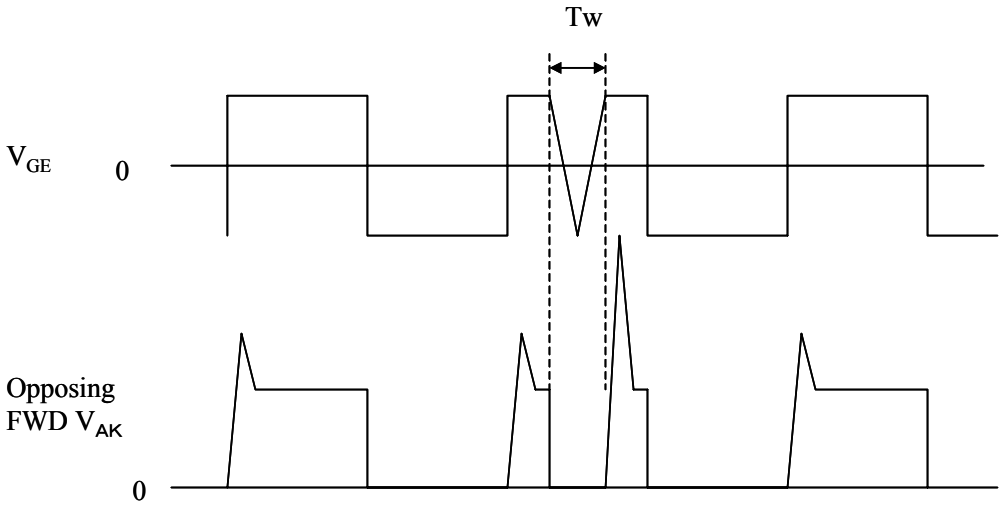
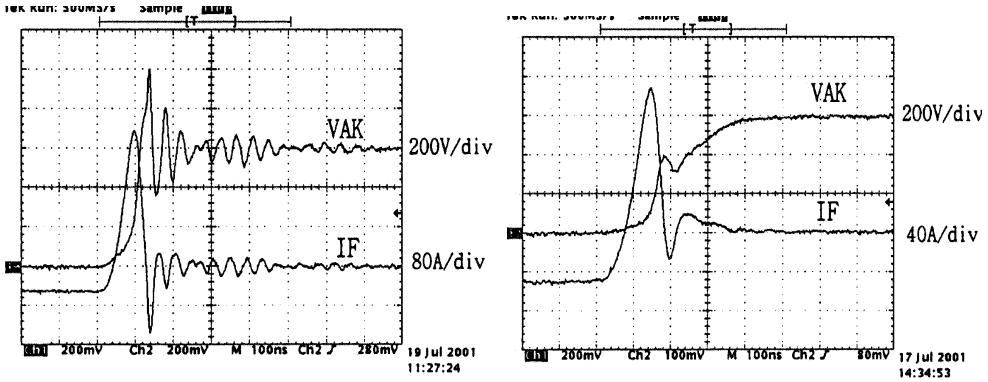


Fig. 4-10 Waveforms at short off pulse reverse recovery

Fig. 4-10 shows a timing chart in which an excessive surge voltage arises from short off pulse reverse recovery. According to this phenomenon, an extremely excessive reverse recovery surge voltage arises between C and E of the FWD on the opposing arm when very short off pulses (Tw) like those shown are generated after gate signal interruptions resulting from noise interferences during IGBT switching. A surge voltage exceeding the guaranteed rated withstand voltage level of the module is most likely to lead to device destruction. Testing has confirmed a sharp increase in surge voltage

when Tw < 1μs. Be sure not to design a circuit that will generate such short gate signal off pulses. This phenomenon occurs because the FWD enters a state of reverse recovery very shortly after it is turned on, so that voltage application begins without a sufficient quantity of carrier stored in the FWD, with the depletion layer spreading rapidly to generate steep di/dt and dv/dt.
With devices supporting an operation mode in which Tw is 1μs or shorter, verify that the surge voltage in the minimum period of Tw does not exceed the device withstand voltage. If the surge voltage exceeds the device withstand voltage rating, take action to reduce surge voltages, such as increasing the R_G, cutting the circuit inductance, building up the snubber circuit or installing a C_{GE}.
Fig. 4-11 shows the diode reverse-recovery waveforms when a short off pulse of 6MBI450U-120 (1200V, 450A). As shown below, surge voltage can be decreased by enlarging R_G from 1.0Ω to 5.6Ω.



(1) Ron=1.0Ω (2) Ron=5.6Ω

Ed=600V, IF=50A, Tj=125°C, Tw=1μs

6MBI450U-120

Fig. 4-11 Waveforms of reverse recovery at short off pulse

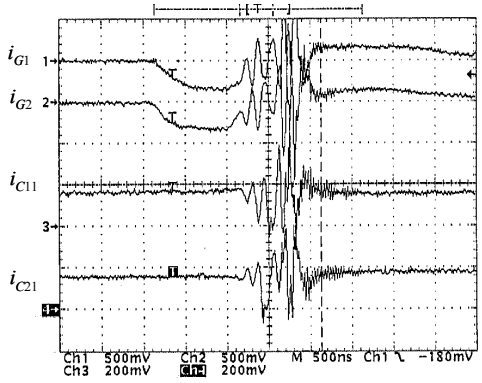
3.5 Oscillation from IGBTs connected in parallel

When products are connected in parallel, the uniformity of the main circuit wiring is very important. Without balanced wiring, concentrated transient currents could occur on the device having a shorter wiring path during switching, which could cause device destruction or degrade long-term reliability. In a main wiring circuit in which the wiring is not uniform or balanced the overall main circuit inductance will also be out of balance among the devices.

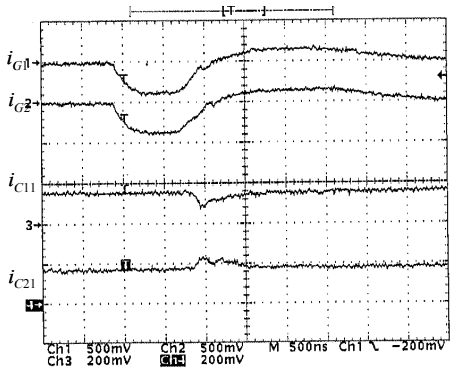
Consequently, voltages of varied potentials are generated in the individual wiring inductances from di/dt during switching, producing an abnormal oscillating current, such as a loop current, leading to possible device destruction.

Fig. 4-12(1) shows the oscillation phenomenon when the wiring inductance of the emitter portion is made extremely unbalanced. An IGBT can generate this oscillation current at the wiring loop in the emitter portion connected in parallel, this influences the gate voltage and the oscillation phenomenon which is generated by the high speed switching. A ferrite core (common mode) can be inserted in each gate emitter wiring circuit to reduce or eliminate the loop current in the emitter portion. Fig. 4-12(2) shows the waveforms with the common mode core. Note the elimination of the previous oscillation.

Give full consideration to maintaining circuit uniformity when designing main circuit wiring.



(1) When emitter inductance is unbalanced



(2) When the common mode core is inserted in gate emitter wiring

i_{G1}, i_{G2}:5A/div, i_{C11}, i_{C21}:100A/div, t:0.5μs/div, Ed=600V 1200V, 300A IGBT 2 parallel connection

Fig. 4-12 Waveforms of 2 parallel connection

3.6 Notes on the soldering process

Problems, such as melting case resin material, could result if excessive soldering temperature is applied when soldering a gate driver circuit or control circuit to the terminals of the IGBT module. Stay within normal soldering processes, avoid high exposure that exceeds maximum recommended terminal soldering defined in the specifications. (Terminal heat resistance test conditions that are covered in the general product specifications documents are listed below for reference.)

Solder temperature: 260±5°C
Dwell time: 10±1s
Cycles: 1

3.7 IGBT Module converter application

Diodes used in the IGBT modules have an I^2t rating. I^2t is a scale of the forward, non-repetitive overcurrent capability of current pulses having a very short duration (less than 10ms). Current (I) denotes the effective current, and time (t) indicates the pulse duration. If the IGBT module is used in a rectifier circuit (or converter circuit), do not exceed the maximum I^2t limits. If you approach the I^2t limits, insert a starter circuit having a resistance and a contactor connected in parallel, for example, between the AC power supply and the IGBT module. If fuse protection is used, select a fuse not exceeding rated I^2t.

3.8 Power cycle life

The IGBT module has a power cycle life as shown in Fig. 4-13. Use the IGBT module below its defined power cycle life. There are two types of power cycle life: ΔTj power cycle and ΔTc power cycle. The ΔTj power cycle raises and lowers the junction temperature at relatively short intervals of time as shown in Fig. 4-13. It is mainly carried out to evaluate the useful life of aluminum wire junctions and soldered joints under the silicon chip.

We continue to pursue the development of IGBT's with longer cycle capability by investigating strains found in soldered joints under thermal stress analyses and mechanisms of destruction associated with differences in ΔTj. The major type of destruction at ΔTj of 100 °C or above is the shearing stress originating from differences in the coefficient of expansion between the silicon chip and the aluminum wire, producing cracks in the junction interface.

The typical destruction at ΔTj of 80°C or lower stems from the shearing stress originating from differences in the coefficient of linear expansion between the silicon chip and the DCB, which produces cracks in the soldered joints. As the cracks progress, the junction temperature rises to cause device destruction.

Because the IGBT module is generally used in a relatively low temperature region in which ΔTj is 80°C or lower, longer-lived soldered junctions are essential to improve the power cycle life. An SnAg-based lead-free solder formulation offering superb mechanical characteristics and wettability has been developed to achieve longer power lives in a relatively low temperature region.

In estimating the power cycle life of an IGBT module used in an actual device, calculate ΔTj in the operating state of the hot device and verify that the power cycle life is longer than the product life time. With a motor driver involving frequent acceleration and decelerations of a motor, for example, maximum junction temperature Tj during acceleration time minus junction temperature Tj during deceleration time gives ΔTj. Determine the power cycle life from ΔTj according to the power cycle immunity shown in Fig. 4-13. Verify that the module power cycle capability is greater than the number of times the device experiences frequent acceleration and deceleration cycles.

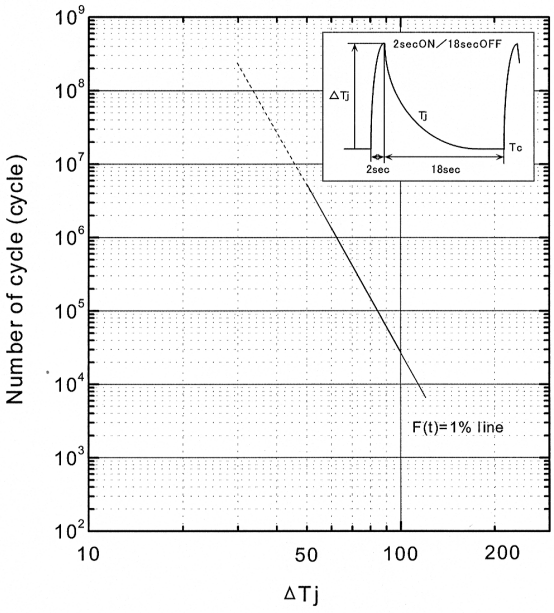


Fig. 4-13 Power cycle life

With a motor drive that runs at a low output frequency, such as 0.5 Hz, determine ΔTj at 0.5 Hz and then the power cycle life from the value of ΔTj. Verify that the power cycle life is longer than the product life time. Further, with the driver involving mixed modes of accelerations and decelerations, and low-speed operations shown in Fig. 4-14, determine ΔTj in each individual operation mode. Then,

verify that the power cycle life determined from each value of ΔTj is longer than the product life time.

3.9 Countermeasure of EMC noise

Amid the ongoing effort to comply with European CE marking for IGBT module-based converters, such as inverters and UPS, and with VCCI regulations in Japan, electromagnetic compatibility (EMC), particularly, holding down noise interferences (conductive and radiating noises emitted from devices in operation) to specifications or below, has become an essential aspect of circuit design.
As IGBT modules continue to offer enhanced characteristics, including faster switching and less loss, from generation to generation, high dv/dt and di/dt generated from their switching action is more frequently becoming a source of radiating noise interferences.

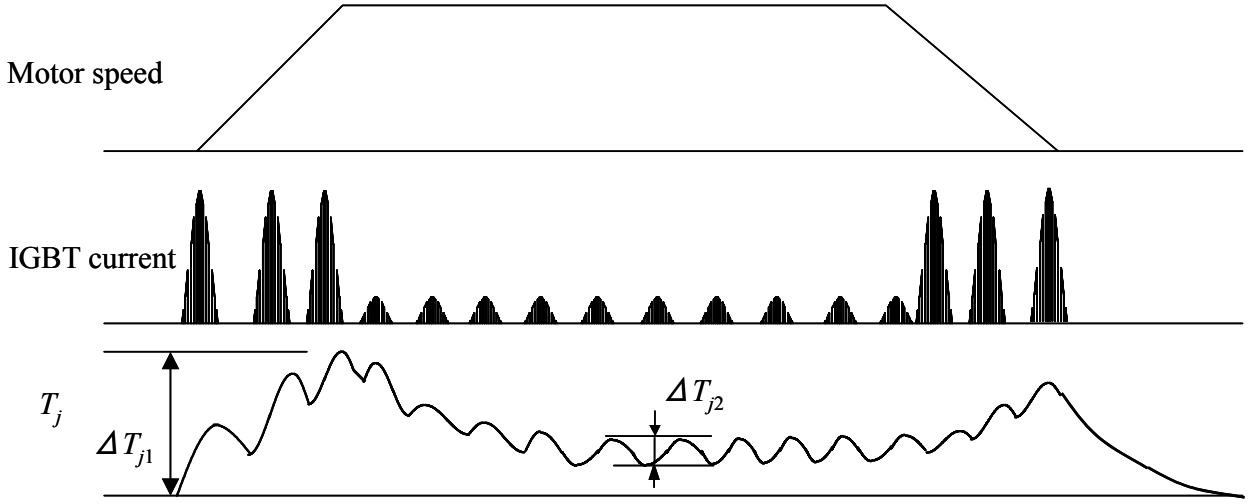
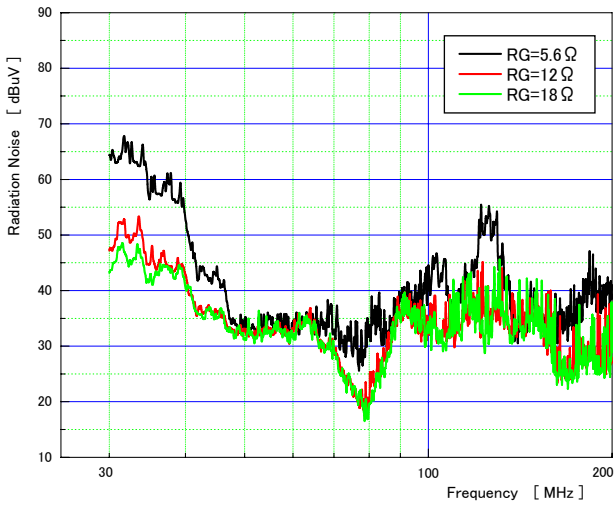


Fig. 4-14 Operations with an actual motor driver (example)

Radiation noises are primarily associated with harmonic LC resonance between stray capacitances, such as semiconductor device junction capacitances, and wiring stray inductances, triggered by high dv/dt and di/dt generated from the IGBTs during turn-on (reverse recovery of the FWD in the opposing arm).

Fig. 4-15 shows examples of radiation noise of 1200V IGBT modules (2MBI150SC-120, 1200V, 150A). The radiation noise with twice standard gate resistance (12Ω) can decrease about 10dB or more.
A soft-waveform implementation of the switching characteristics to decrease radiation noises, however, tends to increase the switching loss. It is important to design the drive conditions to keep them balanced with the device operating conditions, module cooling conditions and other relevant conditions.
Moreover, a general example of countermeasures of radiation noise is shown in Table 4-2. Because the generation factor and noise level are different according to the wiring structure of the device and the material and the circuit composition, etc., it is necessary to verify which of the countermeasures is effective.



Motor driver:15kW, Molule:2MBI150SC-120

Fig. 4-15 Radiation noise of motor drivers

Table 4-2 Countermeasures of radiation noise

Action	Description	Remarks
Review drive conditions (cut dv/dt and di/dt)	Increase the gate resistance (particularly, turn-on side) to two to thee times the standard value listed in the datasheet.	The switching loss increases. The switching time lengthens.
	Insert a small capacitor between the gate and emitter. Its capacitance should be somewhere from the feedback capacitance to the input capacitance (Cres to Cies).	The switching loss increases. The switching time lengthens.
Minimize the wiring between the snubber capacitor and the IGBT module	Minimize the wiring distance between the snubber capacitor and the IGBT module (connect to the module pins).	Also useful for canceling surge voltages during switching and dv/dt.
Cut wiring inductances	Use laminated bus bars to reduce inductances.	Also useful for canceling surge voltages during switching and dv/dt.
Filtering	Connect noise filters to device input and output.	Various filters are commercially available.
Shield wirings	Shield the I/O cables to cut radiating noise from the cables.	
Metalize the device case	Metalize the device cabinet to suppress noise emissions from the device.	

Chapter 5
Protection Circuit Design

CONTENTS **Page**

This section explains the protection circuit design.

1 Short circuit (overcurrent) protection

1.1 Short circuit withstand capability

In the event of a short circuit, first the IGBT's collector current will rise, once it has reached a certain level, the C-E voltage will spike. Depending on the device's characteristics, during the short-circuit, the collector current can be kept at or below a certain level, however the IGBT will still continue to be subjected to a heavy load (high voltage and high current).
Therefore, this condition must be removed as soon as possible. The amount of time allowed between the start of a short circuit until the current is cut off, is limited by the IGBT's short circuit withstand capability.
The short-circuit withstand capability, as illustrated in Fig. 5-1. It is determined by the amount of time it takes from the start of the short-circuit current until the module is destroyed. The withstand capability of the N series IGBTs is as follows:

Short-circuit withstand capability: 10μs minimum

< Conditions >

· **V_{CC} 600V series: Ed(V_{CC})=400V**
1200V series: Ed(V_{CC})=800V
· **V_{GE} = 15V**
· **R_G: Standard R_G value** (from the specifications)
· **T_j = 125°C**

In general, the higher the supply voltage (Ed) or temperature (T_j) rises, the lower the short-circuit withstand capability.

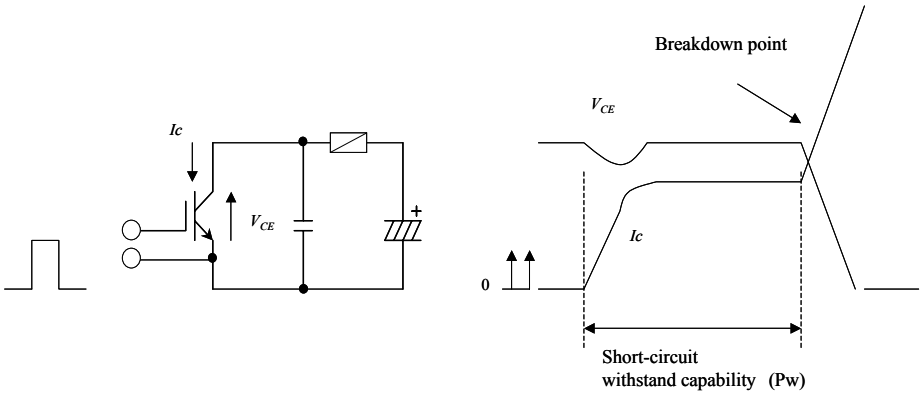
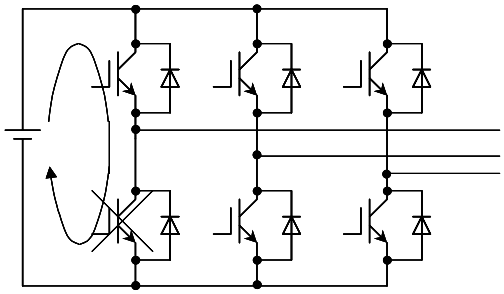
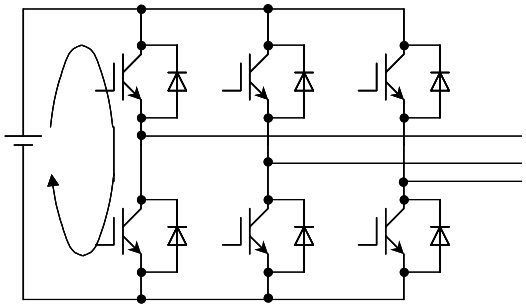
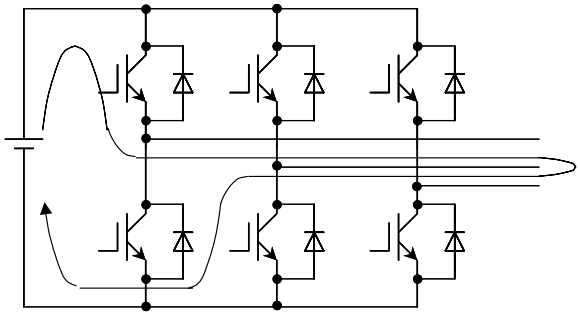
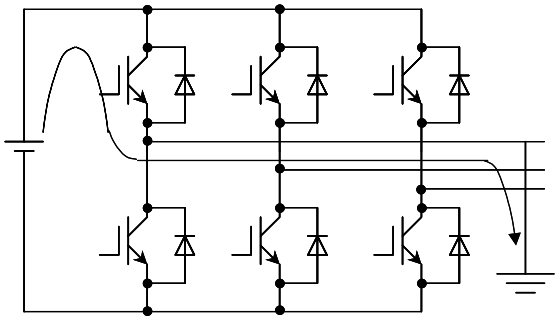


Fig. 5-1 Measuring circuit and waveform

1.2 Short-circuit modes and causes

Table 5-1 lists the short-circuit modes and causes that occur in inverters.

Table 5-1 Short circuit mode and cause

Short circuit mode	Cause
Arm short circuit 	Transistor or diode destruction
Series arm short circuit 	Faulty control/drive circuit or noise induce malfunction
Short in output circuit 	Miswiring or dielectric breakdown of load
Ground fault 	Miswiring or dielectric breakdown of load

1.3 Short-circuit (overcurrent) detection

1) Detection in the circuit

As stated previously, in the event of a short-circuit, the IGBT must be disabled as soon as possible. Therefore, the time from overcurrent detection to the complete turn-off in each circuit must be as short as possible.

Since the IGBT turns off very quickly, if the overcurrent is shut off using an ordinary drive signal, the collector-emitter voltage will rise due to the inductive kick, and the IGBT may be destroyed by overvoltage (RBSOA destructions). Therefore, it is recommended that when cutting off the overcurrent that the IGBT be turned off gently (Soft turn-off).

Figure 5-2 shows the insertion methods for overcurrent detectors, and Table 5-2 lists the features of the various methods along with their detection possibilities. After determining what kind of protection is necessary, select the most appropriate form of detection.

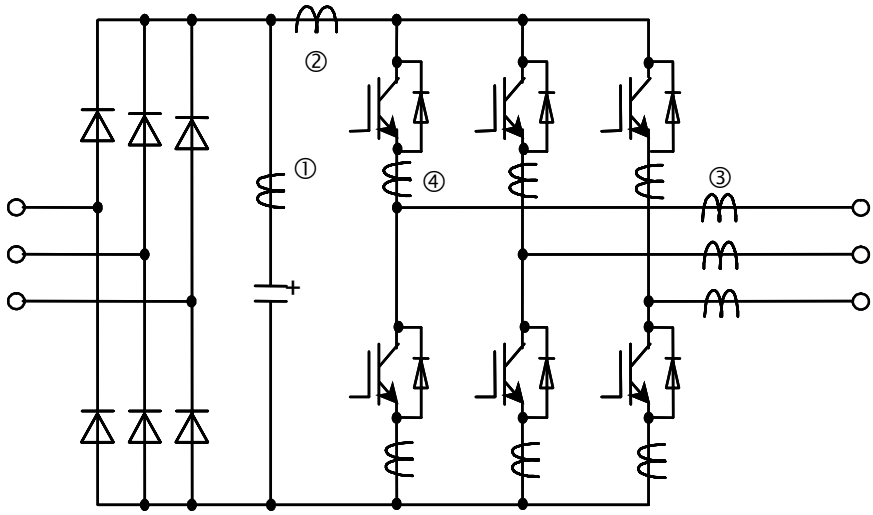


Fig. 5-2 Overcurrent detector insertion methods

Table 5-2 Overcurrent detector insertion positions and function

Detector insertion position	Features	Detection function
Insertion in line with smoothing capacitor Fig. 5-2/①	• AC current transformer available • Low detection precision	• Arm short-circuit • Short in output circuit • Series arm short-circuit • Ground fault
Insertion at inverter input Fig. 5-2/②	• Necessary to use DC current transformer • Low detection precision	• Arm short-circuit • Short in output circuit • Series arm short-circuit • Ground fault
Insertion at inverter output Fig. 5-2/③	• AC current transformer available for high frequency output equipment • High detection precision	• Short in output circuit • Ground fault
Insertion in line with switches Fig. 5-2/④	• Necessary to use DC current transformer • High detection precision	• Arm short-circuit • Short in output circuit • Series arm short-circuit • Ground fault

2) Detecting using $V_{CE(sat)}$

This method can protect against all of the short-circuit types listed in Table 5-1. Since all operations from overcurrent detection to protection are done on the drive circuit side, this offers the fastest protection possible. A short-circuit protection schematic, based in $V_{CE(sat)}$ detection, is shown in Fig. 5-3.

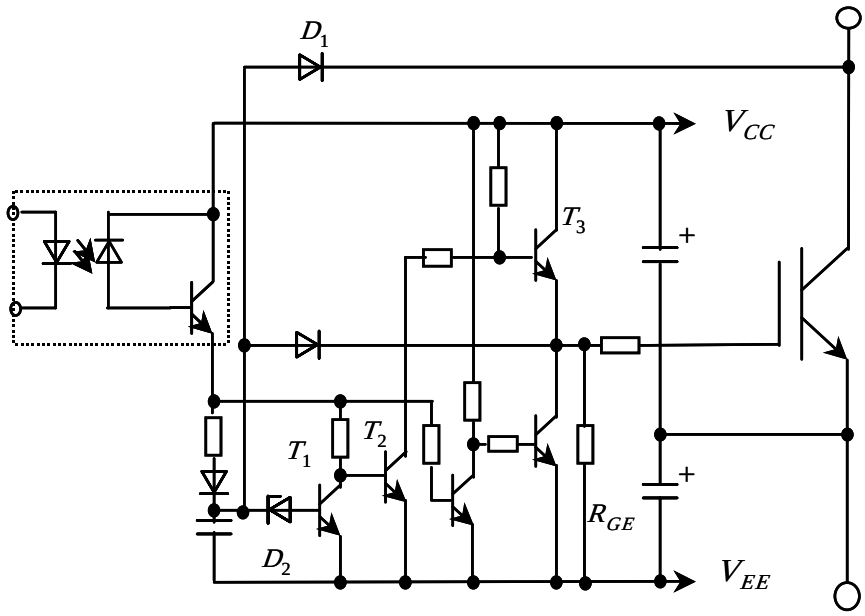
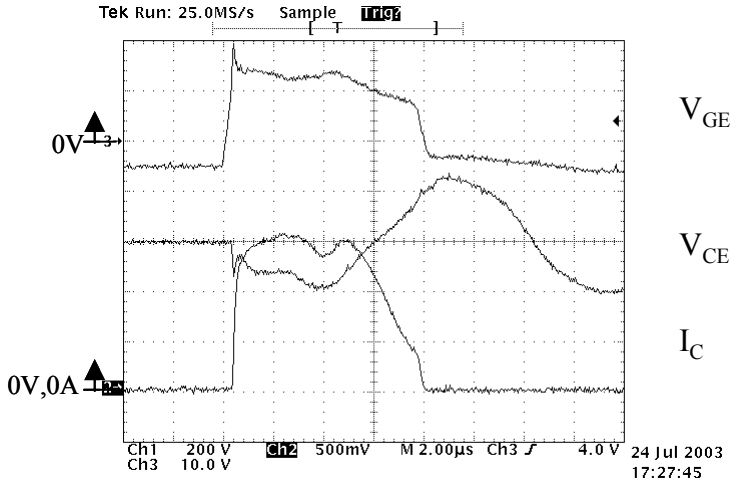


Fig. 5-3 Shirt-circuit protection schematic based in V_{CE}(sat) detection

This circuit uses D_1 to constantly monitor the collector-emitter voltage, so if during operation the IGBT's collector-emitter voltage rises above the limit at D_2, then a short-circuit condition will be detected and T1 will be switched on while T_2 and T_3 are switched off. At this time, the accumulated charge at the gate is slowly released through the R_{GE}, so a large voltage spike is prevented when the IGBT is turned off.

Fuji Electric's gate driver hybrid IC_S (model EXB840, 841) have the same kind of protective circuit built in, thereby simplifying the drive circuit design. For more details, refer to Chapter 7 "Drive Circuit Design". Fig. 5-4 shows an IGBT waveform during short circuit protection.



2MBI300UD-120

Ed=600V, V_{GE}=+15V, –5V (EXB841), R_G=3.3Ω, Tj=125°C

V_{CE}=200V/div, I_C=250A, V_{GE}=10V/div, t=2µs/div

Fig. 5-4 Waveforms during short circuit protection

2 Overvoltage protection

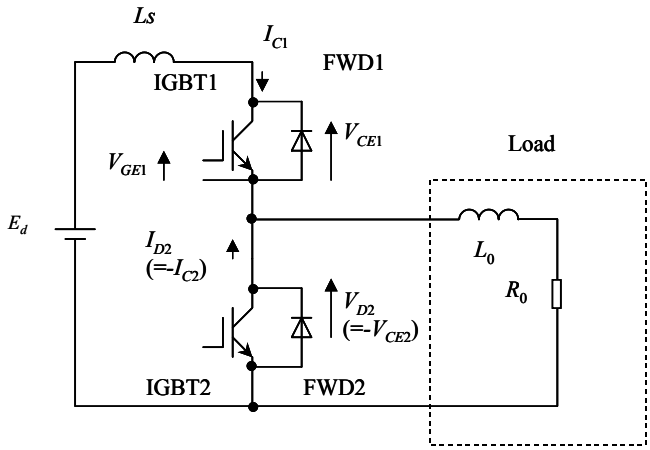
2.1 Overvoltage causes and their suppression

1) Overvoltage causes

Due to the high switching speed of IGBTs, at turn-off or during FWD reverse recovery, the current change rate (di/dt) is very high. Therefore the circuit wiring inductance to the module can cause a high turn-off surge voltage (V=L(di/dt)).

At an example, using the IGBT's waveform at turn-off we will introduce the causes and methods of their suppression, as well as illustrate a concrete example of a circuit (using an IGBT and FWD together).

To demonstrate the turn-off surge voltage, a simplified chopper circuit is shown in Fig. 5-5, and the IGBT turn-off voltage and current waveforms are shown in Fig. 5-6.



E_d: DC supply voltage, L_S: Main circuit wiring inductance, Load:L_0,R_0

Fig. 5-5 Chopper circuit

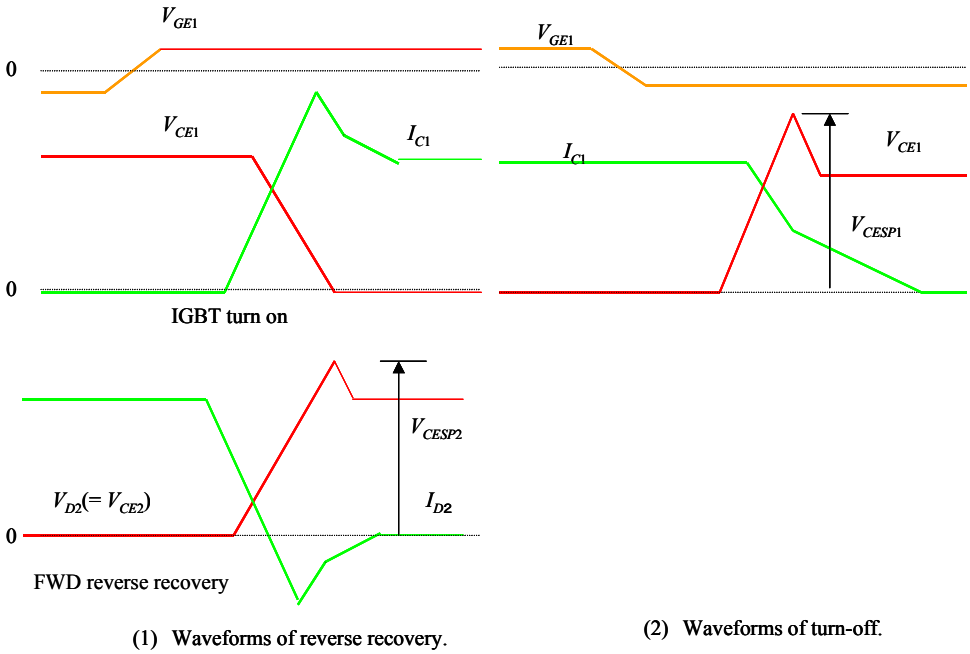


Fig. 5-6 Switching waveforms

The turn-off surge voltage peak V_{CESP} can be calculated as follows:

$$V_{CESP} = Ed + (-L_S \bullet dIc/dt) \cdots\cdots\cdots\cdots\cdots\cdots \text{①}$$

dIc/dt: Maximum collector current change rate at turn-off

If V_{CESP} exceeds the IGBT's C-E (V_{CES}) rating, then the module will be destroyed.

2) Overvoltage suppression methods

Several methods for suppressing turn-off surge voltage, the cause for overvoltage, are listed below:

a. Control the surge voltage by adding a protection circuit (snubber circuit) to the IGBT.
   Use a film capacitor in the snubber circuit, place it as close as possible to the IGBT in order to bypass high frequency surge currents.
b. Adjust the IGBT drive circuit's $-V_{GE}$ or R_G in order to reduce the di/dt value. (Refer to Chapter 7, "Drive Circuit Design".)
c. Place the electrolytic capacitor as close as possible to the IGBT in order to reduce the effective inductance of the wiring. Use a low impedance capacitor.
d. To reduce the inductance of the main as well as snubber circuit's wiring, use thicker and shorter wires. It is also very effective to use laminated copper bars in the wring.

2.2 Types of snubber circuits and their features

Snubber circuits can be classified into two types: individual and lump. Individual snubber circuits are connected to each IGBT, while lump snubber circuits are connected between the DC power-supply bus and the ground for centralized protection.

1) Individual snubber circuits

Examples of typical individual snubber circuits are listed below.

a) RC snubber circuit
b) Charge and discharge RCD snubber circuit
c) Discharge-suppressing RCD snubber circuit

Table 5-3 shows the schematic of each type of individual snubber circuit, its features, and an outline of its main uses.

2) Lump snubber circuits

Examples of typical snubber circuits are listed below.

a) C snubber circuits
b) RCD snubber circuits

Lump snubber circuits are becoming increasingly popular due to circuit simplification.
Table 5-4 shows the schematic of each type of lump snubber circuit, its features, and an outline of its main applications. Table 5-5 shows the capacity selection of a C type snubber circuit. Fig. 5-7 shows the current and voltage turn-off waveforms for an IGBT connected to a lump snubber circuit.

Table 5-3 Individual snubber circuits

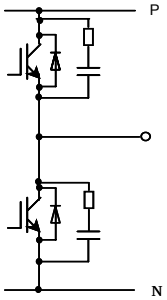
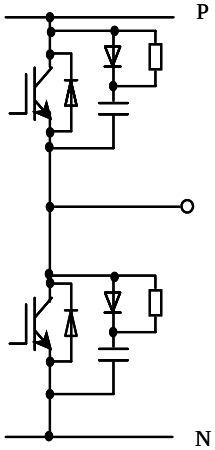
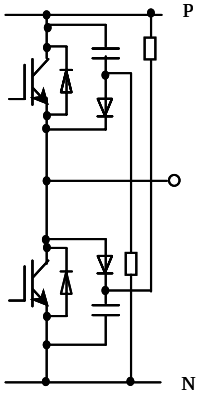
Snubber circuit schematic	Circuit features (comments)	Main application
RC snubber circuit 	• The effect on turn-off surge voltage suppression is great. • Perfect for chopper circuits • When applied to large capacity IGBTs, the snubber's resistance must be low. Consequently however, the above makes the load conditions at turn-on more severe.	Arc welder Switching power supply
Charge and discharge RCD snubber circuit 	• The effect on turn-off surge voltage is moderate. • As opposed to the RC snubber circuit, a snubber diode has been added. This allows the snubber's resistance to increase and consequently avoids the IGBT load conditions at turn-on problem. • Since the power dissipation loss of this circuit (primarily caused by the snubber's resistance) is much greater than that of a discharge suppressing snubber circuit, it is not considered suitable for high frequency switching applications. • The power dissipation loss caused by the resistance of this circuit can be calculated as follows: $P = \frac{L \bullet Io^2 \bullet f}{2} + \frac{C_s \bullet Ed^2 \bullet f}{2}$ L: Wiring inductance of main circuit, Io: Collector current at IGBT turn-off, Cs: Capacitance of snubber capacitor, Ed: DC supply voltage, f :Switching frequency	
Discharge suppressing RCD snubber circuit 	• The effect on turn-off surge voltage is small • Suitable for high-frequency switching • Power dissipation loss caused by snubber circuit is small. • The power dissipation loss caused by the resistance of this circuit can be calculated as follows: $P = \frac{L \bullet Io^2 \bullet f}{2}$ L: Wiring inductance of main circuit Io: Collector current at IGBT turn-off f :Switching frequency	Inverter

Table 5-4 Lump snubber circuits

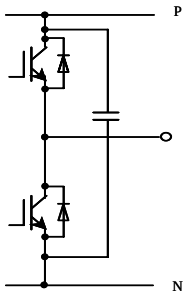
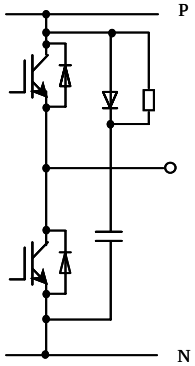
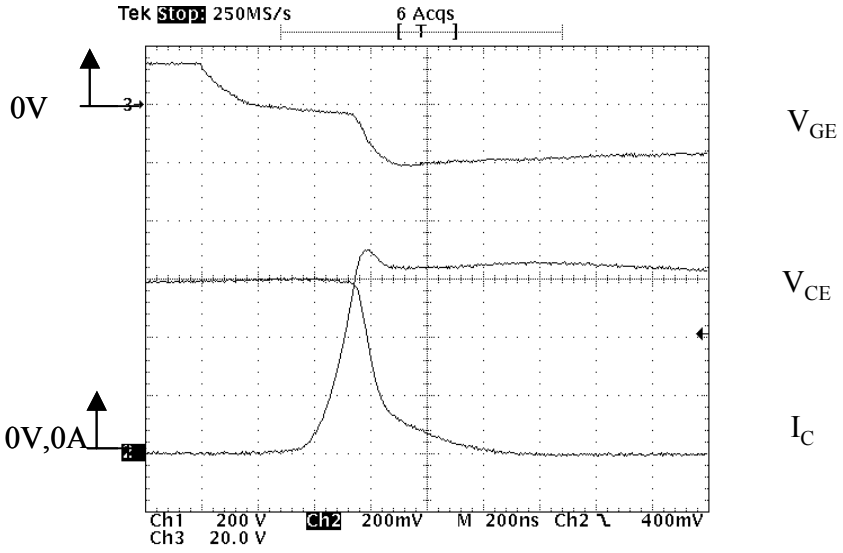
Snubber circuit schematic	Circuit features (comments)	Main application
C snubber circuit 	• This is the simplest circuit • The LC resonance circuit, which consists of a main circuit inductance coil and snubber capacitor, may cause the C-E voltage to oscillate.	Inverter
RCD snubber circuit 	• If the wrong snubber diode is used, a high spike voltage will be generated and the output voltage will oscillate at the diodes reverse recovery.	Inverter

Table 5-5 Guidelines for determining lump C snubber circuit capacity

Module rating \ Item		Drive conditions[*1]		Main circuit wiring inductance (μH)	Capacitance of snubber capacitance Cs (μF)
		$-V_{GE}$(V)	R_G(Ω)		
600V	50A	15 max.	68 min.	-	0.47
	75A		47 min.		
	100A		33 min.		
	150A		24 min.	0.2 max.	1.5
	200A		16 min.	0.16 max.	2.2
	300A		9.1 min.	0.1 max.	3.3
	400A		6.8 min.	0.08 max.	4.7
1200V	50A	15 max.	22 min.	-	0.47
	75A		9.1 min.		
	100A		5.6 min.		
	150A		4.7 min.	0.2 max.	1.5
	200A		3.0 min.	0.16 max.	2.2
	300A		2.0 min.	0.1 max.	3.3

*[1]: Typical standard gate resistance of U series IGBT is shown.



6MBI300U-120
Ed=600V, V_{GE}=+-15V, Ic=300A, R_G=2.2Ω, Tj=125C, Ls=65nH
V_{CE}: 200V/div, I_C: 100A/div, V_{GE}: 20V/div, t: 200ns/div

Fig. 5-7 Current and voltage waveforms of IGBT in lump snubber circuit at turn-off

2.3 Discharge-suppressing RCD snubber circuit design

The discharge suppressing RCD can be considered the most suitable snubber circuit for IGBTs. Basic design methods for this type of circuit are explained in the following.

1) Study of applicability

Figure 5-8 is the turn-off locus waveform of an IGBT in a discharge-suppressing RCD snubber circuit. Fig. 5-9 shows the IGBT current and voltage waveforms at turn-off.

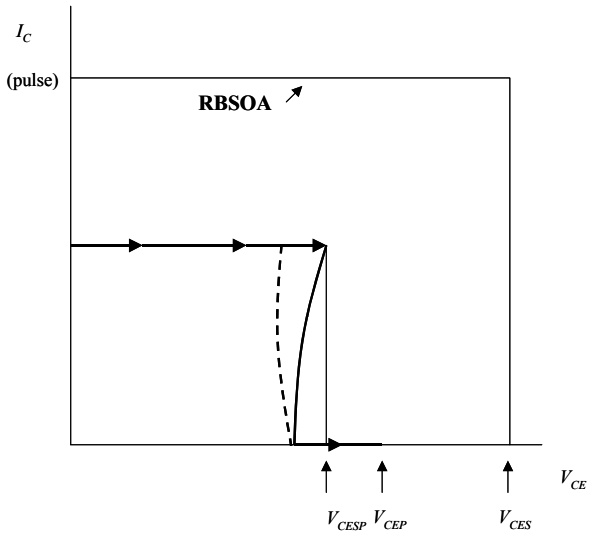


Fig. 5-8 Turn-off locus waveform of IGBT

The discharge-suppressing RCD snubber circuit is activated when the IGBT C-E voltage starts to exceed the DC supply voltage. The dotted line in diagram Fig. 5-8 shows the ideal operating locus of an IGBT. In an actual application, the wiring inductance of the snubber circuit or a transient forward voltage drop in the snubber diode can cause a spike voltage at IGBT turn-off. This spike voltage causes the sharp-cornered locus indicated by the solid line in Fig. 5-8.
The discharge-suppressing RCD snubber circuits applicability is decided by whether or not the IGBTs operating locus is within the RBSOA at turn-off.

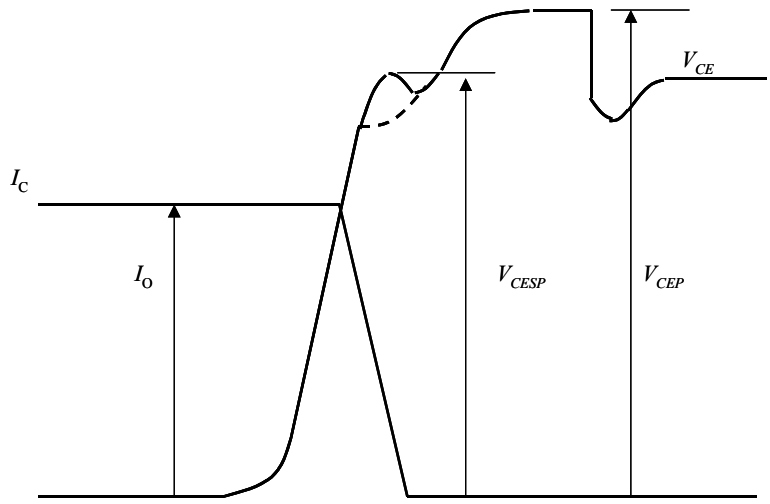


Fig. 5-9 Voltage and current waveforms at turn-off

The spike voltage at IGBT turn-off is calculated as follows:

$$V_{CESP} = Ed + V_{FM} + (-L_S \bullet dIc/dt) \cdots\cdots\cdots\cdots ②$$

Ed: Dc supply voltage
V_{FM}: Transient forward voltage drop in snubber diode
The reference values for the transient forward voltage drop in snubber diodes is as follows:
600V class: 20 to 30V
1200V class: 40 to 60V
Ls: Snubber circuit wiring inductance
dIc/dt: Maximum collector current change rate a IGBT turn-off

2) Calculating the capacitance of the snubber capacitor (Cs)

The necessary capacitance of a snubber capacitor is calculated as follows:

$$C_S = \frac{L \bullet Io^2}{(V_{CEP} - Ed)^2} \cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots ③$$

L: Main circuit wiring inductance
Io: Collector current at IGBT turn-off
VCEP: Snubber capacitor peak voltage
Ed: DC supply voltage

VCEP must be limited to less than or equal to the IGBT C-E withstand voltage.

3) Calculating Snubber resistance (Rd)

The function required of snubber resistance is to discharge the electric charge accumulated in the

snubber capacitor before the next IGBT turn-off.
To discharge 90% of the accumulated energy by the next IGBT turn-off, the snubber resistance must be as follows:

$$R_S \leq \frac{1}{2.3 \bullet C_S \bullet f} \quad \cdots\cdots ④$$

f: Switching frequency

If the snubber resistance is set too low, the snubber circuit current will oscillate and the peak collector current at the IGBT turn-off will increase. Therefore, set the snubber resistance in a range below the value calculated in the equation.
Irrespective of the resistance, the power dissipation loss P (Rs) is calculated as follows:

$$P(R_S) = \frac{L \bullet Io^2 \bullet f}{2} \quad \cdots\cdots ⑤$$

4) Snubber diode selection

A transient forward voltage drop in the snubber diode is one factor that can cause a spike voltage at IGBT turn-off.
If the reverse recovery time of the snubber diode is too long, then the power dissipation loss will also be much greater during high frequency switching. If the snubber diode's reverse recovery is too hard, then the IGBT C-E voltage will drastically oscillate.

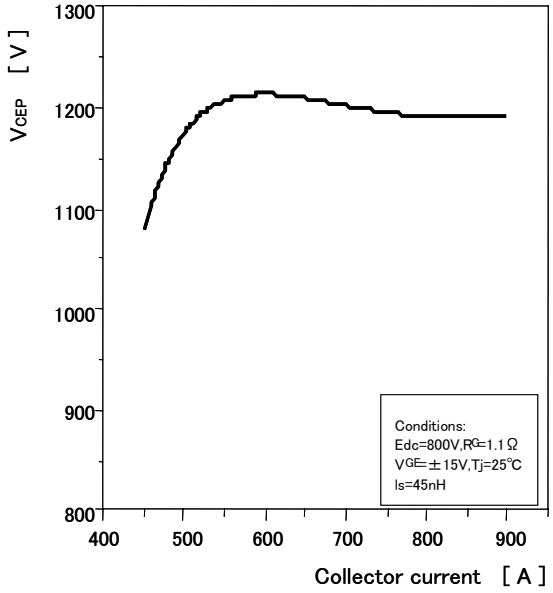
Select a snubber diode that has a low transient forward voltage, short reverse recovery time and a soft recovery.

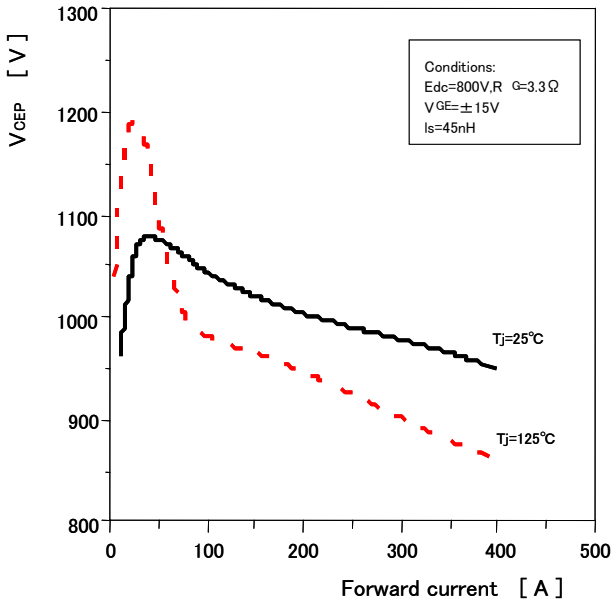
5) Snubber circuit wiring precautions

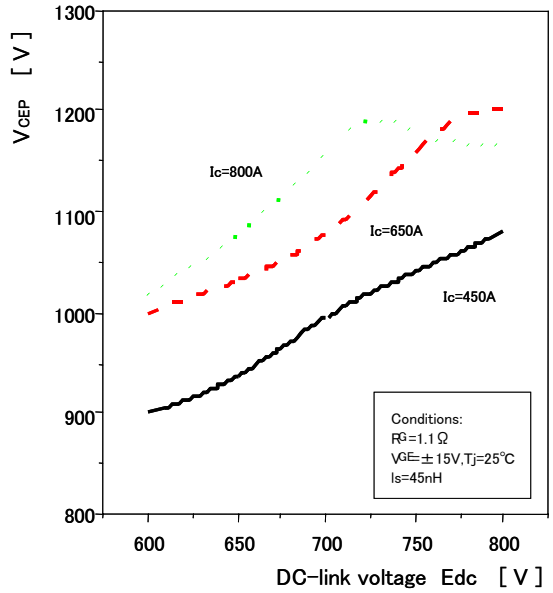
The snubber circuit's wiring inductance is one of the main causes of spike voltage, therefore it is important to design the circuit with the lowest inductance possible.

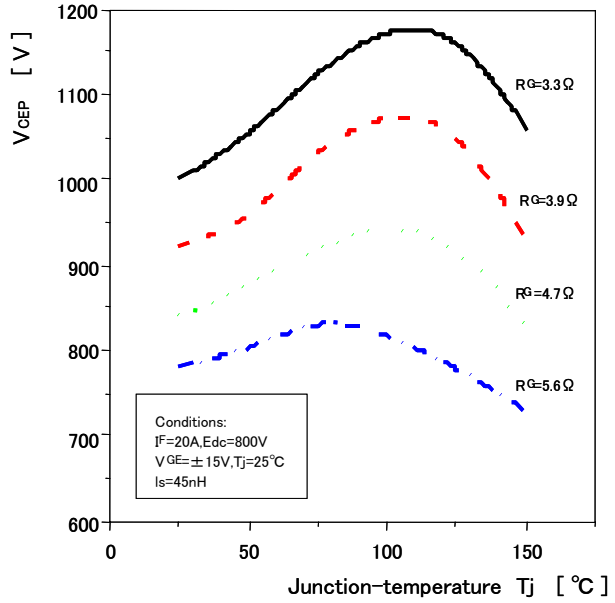
2.4 Example of characteristic of surge voltage

The characteristic of the surge voltage at the turn-off for the U series IGBT (6MBI450U-120) is shown in Fig. 5-10. The larger the turn-off current the greater the turn-off surge voltage. Fig. 5-11 shows the surge voltage of the FWD for the same U series IGBT in reverse recovery. In general, reverse recovery surge voltage becomes large when collector current is approx. 2 to 20% of maximum Ic rating. Suppress recovery surge within RBSOA.









6MBI450U-120

Fig. 5-10 Surge voltage of turn-off

6MBI450U-120

Fig. 5-11 Surge voltage of reverse recovery

Chapter 6
Cooling Design

CONTENTS **Page**

This section explains the cooling design.

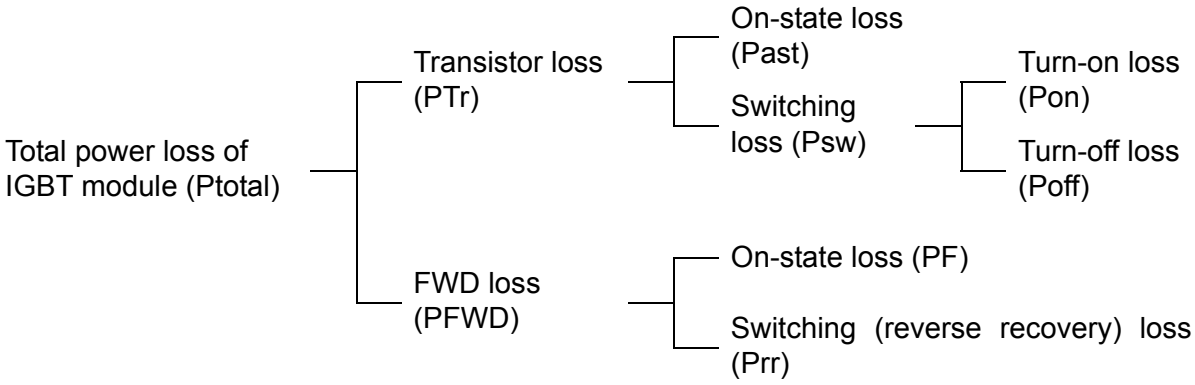
For safe IGBT operation, the junction temperature (Tj) must never exceed Tj(max). Therefore, it is necessary to have a cooling design capable of keeping the junction temperature below Tj(max), even during overload conditions.

1 Power dissipation loss calculation

1.1 Types of power loss

An IGBT module consists of IGBT chips and FWD chips. The sum of the power losses from these sections equals the total power loss for the module. Power loss can be classified as either on-state loss or switching loss. A diagram of the power loss factors is shown as follows.

Power loss factors



The on-state power loss from the IGBT and FWD sections can be calculated using the output characteristics, while switching loss can be calculated from switching loss vs. collector current characteristics. Use these power loss calculations in order to design cooling sufficient to keep the junction temperature Tj below the maximum rated value.
The on-voltage and switching loss values to be used here, are based on the standard junction temperature Tj (125°C is recommended).
For characteristics data, refer to the module specification sheets.

1.2 DC chopper circuit power loss calculations

For easy approximate calculations, consider the current flowing to the IGBT or FWD as a train of square waves. Fig. 6-1 is a diagram showing the approximate waveforms of a DC chopper circuit. At collector current Ic the saturation voltage is represented by $V_{CE(sat)}$ and switching energy is represented by Eon and Eoff. At FWD forward current I_F, V_F represents the on- voltage and E_{RR} represents the energy loss during reverse recovery. Using the above parameters, IGBT power loss can be calculated as follows:

IGBT power dissipation loss (w) = On-state loss + Turn-on loss + Turn-off loss

$$= \left[t1/t2 \times V_{CE(sat)} \times I_C\right] + \left[fc \times \left(E_{on} + E_{off}\right)\right]$$

FWD power dissipation loss (w) = On-state loss + Reverse recovery loss

$$= \left[(1 - (t1/t2)) \times I_F \times V_F\right] + \left[fc \times E_{rr}\right]$$

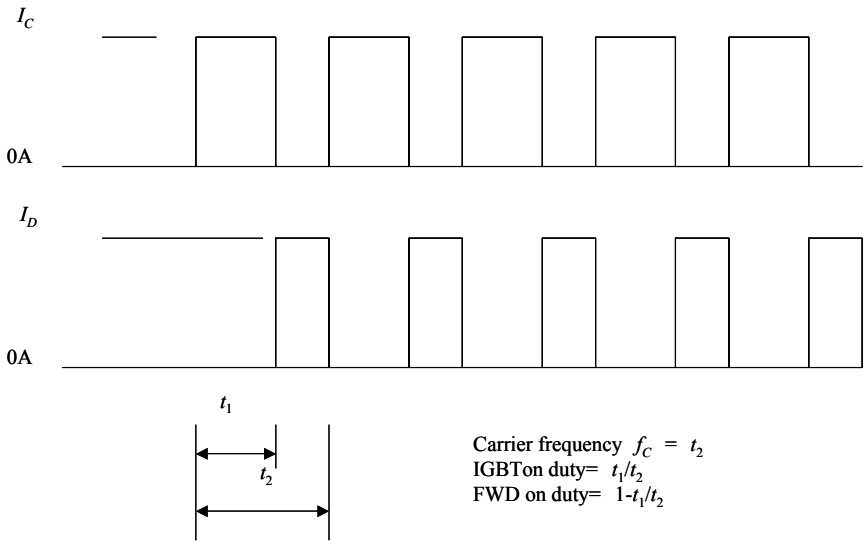


Fig. 6-1 DC chopper circuit current waveforms

The DC supply voltage, gate resistance, and other circuit parameters, may deviate from the standard value listed in the module specification sheets. In this event, approximate values can be calculated according to the following rules:

- DC supply voltage Ed(VCC) deviation
  On voltage: Not dependent on Ed(VCC)
  Switching loss: Proportional to Ed(VCC)

- Gate resistance deviation
  On voltage: Not dependent on gate resistance
  Switching loss: Proportional to switching time and dependent on gate resistance

1.3 Sine-wave VVVF inverter application power dissipation loss calculation

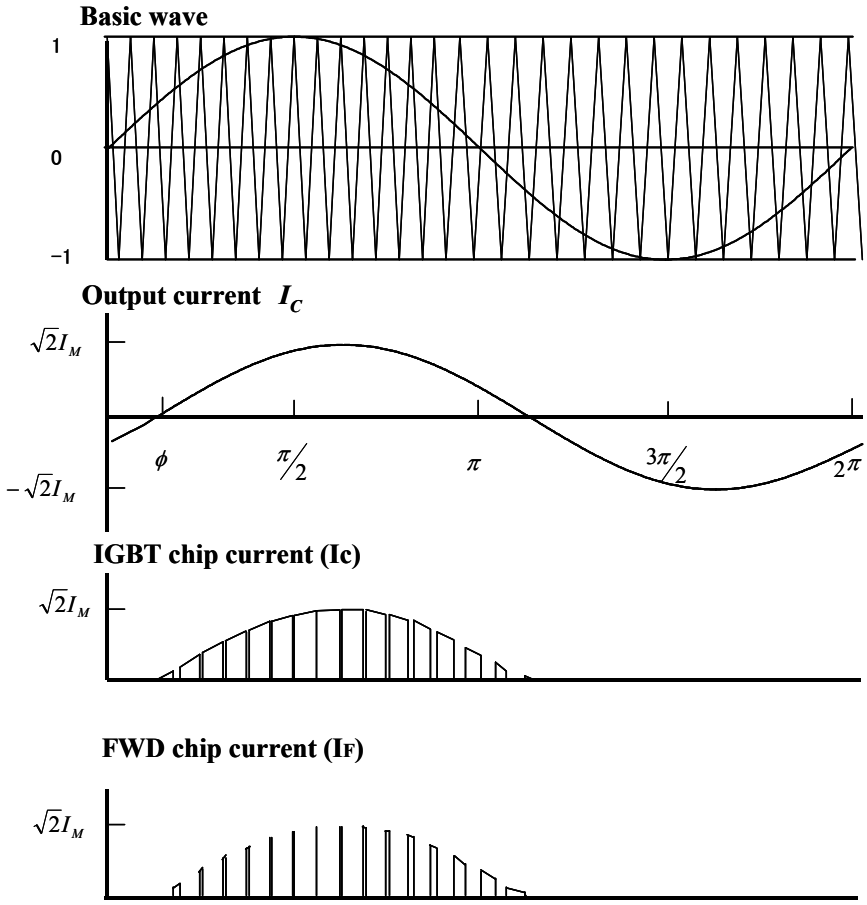


Fig. 6-2 PWM inverter output current

When using a VVVF inverter for a PWM control, the current value and operation keep changing as shown in Fig. 6-2. Therefore, it is necessary to use computer simulations in order to make detailed power loss calculations. However, since computer simulations are very complicated, the following is an explanation of a simple method that generates approximate values.

1) Prerequisites

For approximate power loss calculations, the following prerequisites are necessary:
• Three-phase PWM-control VVVF inverter for sine-wave current output
• PWM control based on the comparison of sine-waves and sawtooth waves
• Output current in ideal sine-wave form

2) Calculating on-state power loss (Psat, P_F)

As displayed in Fig. 6-3, the output characteristics of the IGBT and FWD have been approximated based on the data contained in the module specification sheets.

On-state power loss in IGBT chip (P_{sat}) and FWD chip (P_F) can be calculated as follows:

$$\left(P_{sat}\right) = DT\int_0^X I_C V_{CE(sat)} d\theta$$
$$= \frac{1}{2} DT\left[\frac{2\sqrt{2}}{\pi} I_M V_O + I_{M^2} R\right]$$

$$\left(P_F\right) = \frac{1}{2} DF\left[\frac{2\sqrt{2}}{\pi} I_M V_O + I_{M^2} R\right]$$

DT, DF: Average conductivity of the IGBT and FWD at a half wave of the output current. (Refer to Fig. 6-4)

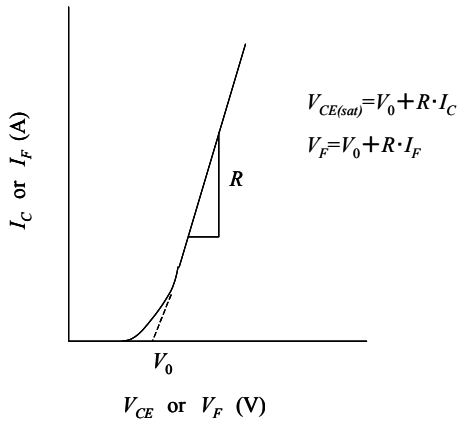


Fig. 6-3 Approximate output characteristics

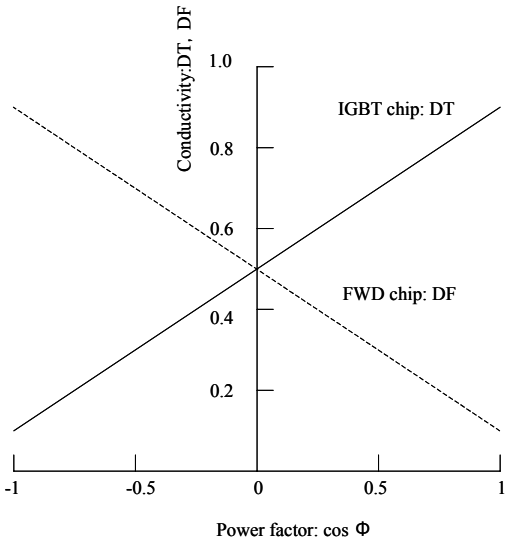


Fig. 6-4 Relationship between power factor sine-wave PWM inverter and conductivity

3) Calculating switching loss

The characteristics of switching loss vs. I_C are generally approximated using the following equations an Fig. 6-5 (Module specification sheet data).

$$E_{on} = E_{on'}\left(I_C / ratedI_C\right)^a$$

$$E_{off} = E_{off'}\left(I_C / ratedI_C\right)^b$$

$$E_{rr} = E_{rr'}\left(I_C / ratedI_C\right)^c$$

a, b, c: Multiplier
Eon', Eoff', Err': Eon, Eoff and Err at rated IC

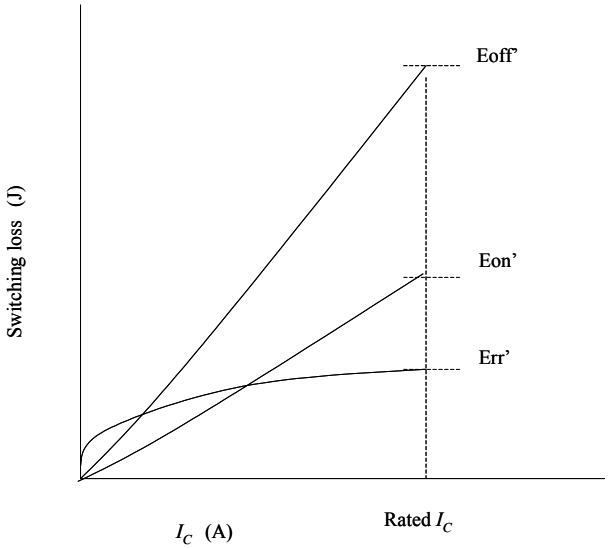


Fig. 6-5 Approximate switching losses

The switching loss can be represented as follows:

• Turn-on loss (P_{on})

$$P_{on} = fo\sum_{K=1}^{n}\left(E_{on}\right)k \qquad \left(n:\ Half-cycle\ switching\ count = \frac{fc}{2fo}\right)$$

$$= foE_{on}'\frac{1}{rated\ I_{C^a}}\sum_{k=1}^{n}\left(I_{C^a}\right)k$$

$$= foE_{on}'\frac{n}{rated\ I_{C^a}\times\pi}\int_0^{\pi}\sqrt{2}I_{M^a}\sin\theta d\theta$$

$$\fallingdotseq foE_{on}'\frac{1}{rated\ I_{C^a}}nI_{M^a}$$

$$= \frac{1}{2}fcE_{on}'\left[\frac{I_M}{rated\ I_C}\right]^a$$

$$= \frac{1}{2}fcE_{on}\left(I_M\right)$$

$E_{on}(IM)$:Ic= E_{on} at I_M

• Turn-off loss (P_{off})

$$P_{off} \fallingdotseq \frac{1}{2}fcE_{off}\left(I_M\right)$$

$E_{off}(I_M)$:Ic= E_{off} at I_M

• FWD reverse recovery loss (P_{rr})

$$P_{off} \fallingdotseq \frac{1}{2} fcE_{rr}(I_M)$$

$E_{rr}(I_M)$:I_c= E_{rr} at I_M

4) Calculating total power loss

Using the results obtained in section 1.3 subsection 2 and 3.

IGBT chip power loss: $P_{Tr} = P_{sat} + P_{on} + P_{off}$

FWD chip power loss: $P_{FWD} = P_F + P_{rr}$

The DC supply voltage, gate resistance, and other circuit parameters will differ from the standard values listed in the module specification sheets.
Nevertheless, by applying the instructions of this section, the actual values can easily be calculated.

2 Selecting heat sinks

Most power diodes, IGBTs, transistors and other power devices are designed to be insulated between electrodes and mounting bases. This type of module can be mounted and wired compactly in a variety of equipment, because several devices can be mounted in a single heat sink. However, in order to ensure safe operation, the power loss (heat) generated by each module must be dissipated efficiently. This is why heat sink selections is very important. The basic of heat sink selection will be illustrated in the following.

2.1 Thermal equations for on-state power loss calculations

The heat conduction of a semiconductor can be simulated in an electric circuit. For this example, with only one IGBT module mounted on the heat sink, the equivalent circuit is shown in Fig. 6-6.

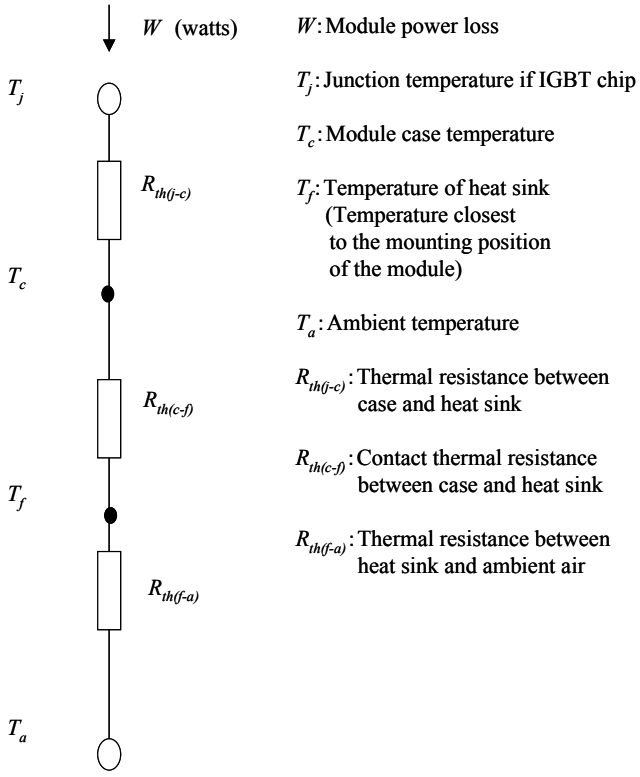


Fig. 6-6 Thermal resistance equivalent circuit

Using the above equivalent circuit, the junction temperature (Tj) can be calculated using the following thermal equation:

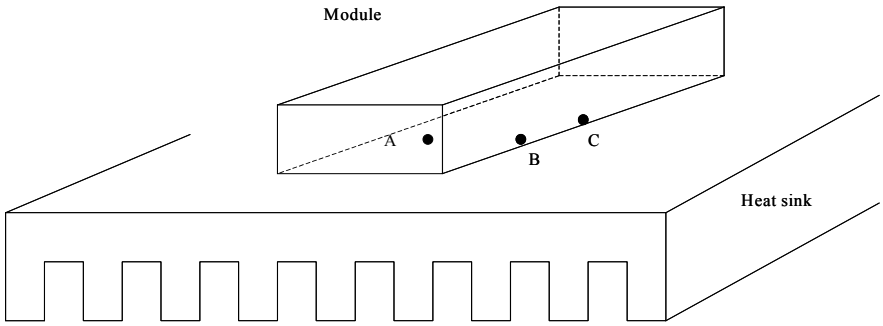
$$Tj = W \times \{Rth(j-c) + Rth(c-f) + Rth(f-a)\} + Ta$$

Note that the case temperature (T_c) and heat sink surface temperature mentioned here are measured from the base of the IGBT module directly below the chip. As shown in Fig. 6-7, the temperature measurements at all other points may be low due to the heat dissipation capability of the heat sink, and this needs to be taken into consideration during final heat sink selection. Next, the equivalent circuit of an IGBT (2-pack-module) and a diode bridge mounted on a heat sink is shown in Fig. 6-8. The thermal equations in this case are as follows:

$$Tj(d) = Wd \times [Rth(j-c)d + Rth(c-f)d] + [(Wd + 2WT + 2WD) \times Rth(f-a)] + Ta$$
$$Tj(T) = WT \times Rth(j-c)T + [(WT + WD) \times Rth(c-f)T] + [(Wd + 2WT + 2WD) \times Rth(f-a)] + Ta$$
$$Tj(D) = WD \times Rth(j-c)D + [(WT + WD) \times Rth(c-f)T] + [(Wd + 2WT + 2WD) \times Rth(f-a)] + Ta$$

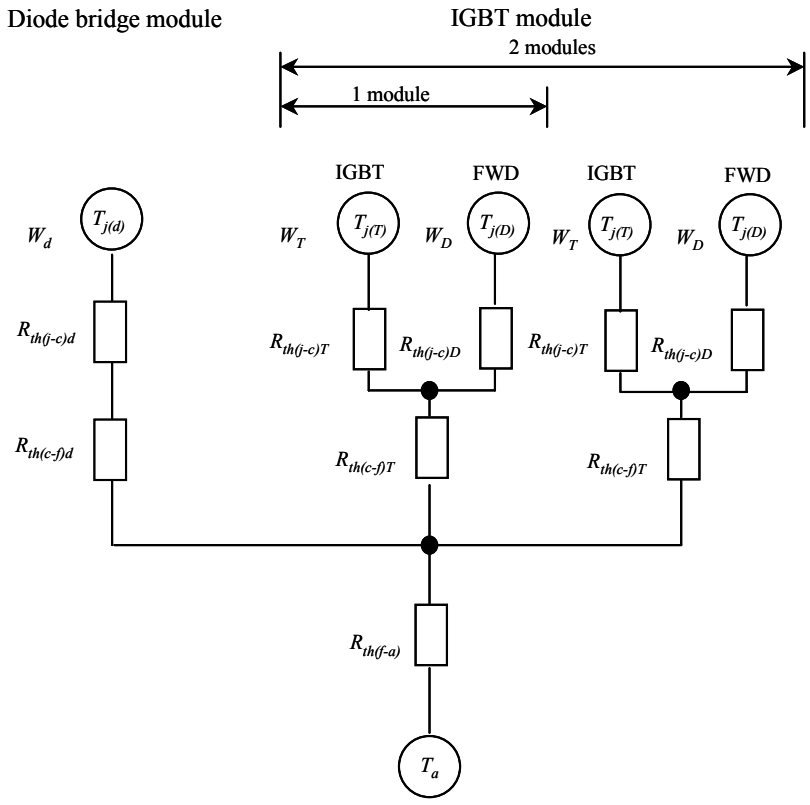
Use the above equations in order to select a heat sink that can keep the junction temperature (T_j) below T_j(max).

A : Directly below the chip by the case
B : Base, 14mm from point A
C : Base, 24mm from point A



	Point A	Point B	Point C
T_C (°C)	51.9	40.2	31.4
T_f (°C)	45.4	36.9	30.2

Fig. 6-7 Example of case and heat sink temperature measurement



W_d, $T_{j(d)}$,$R_{th(\ )d}$: Diode bridge (For one module)

W_T, $T_{j(T)}$, $R_{th(\ )T}$: IGBT (Each element)

W_D, $T_{j(D)}$, $R_{th(\ )D}$: FWD (Each element)

Fig. 6-8 Thermal resistance equivalent circuit

2.2 Thermal equations for transient power loss calculations

In general, as before, it is all right to base the on-state T_j on the average power loss. However, in actuality, repetitive switching causes power loss to pulse and the occurrence of temperature ripples as shown in Fig. 6-10.
First consider the power loss as a train of constant cycles, and constant-peak square pulses. Then calculate the approximate peak of the temperature ripples using the transient thermal resistance curve given in the module specification sheets.
Be certain to select a heat sink that will also keep the T_{jp} below T_j (max).

$$Tjp - T_C = P \times \left[R(\infty) \times \frac{t1}{t2} + \left(1 - \frac{t1}{t2}\right) \times R(t1+t2) - R(t2) + R(t1) \right]$$

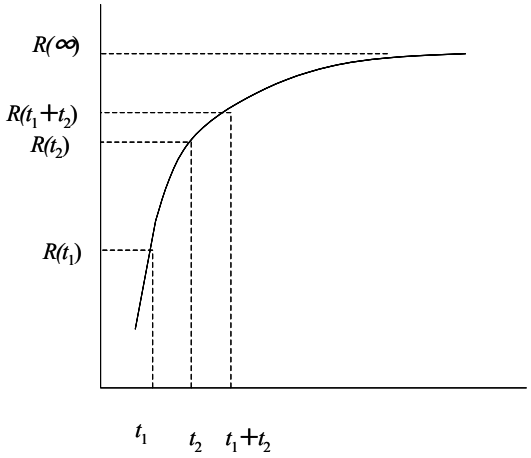


Fig. 6-9 Transient thermal resistance curve

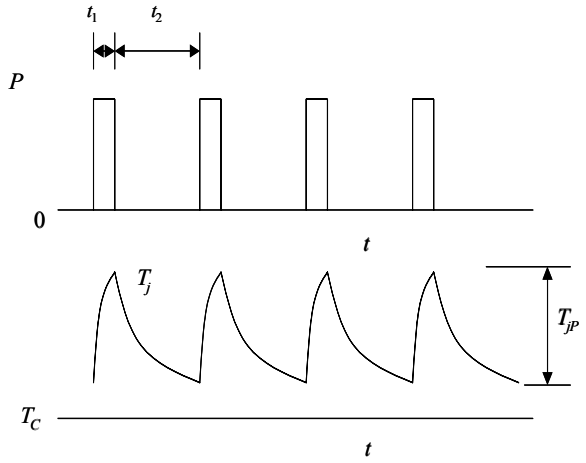


Fig. 6-10 Thermal ripples

3 Heat sink mounting precautions

3.1 Heat sink mounting

Since thermal resistance varies according to an IGBT's mounting position, pay attention to the following points:

- When mounting only one IGBT module, position it in the exact center of the heat sink in order to minimize thermal resistance.
- When mounting several IGBT modules, determine the individual position on the heat sink according to the amount of heat that each module generates. Allow more room for modules that generate more heat.

3.2 Heat sink surface finishing

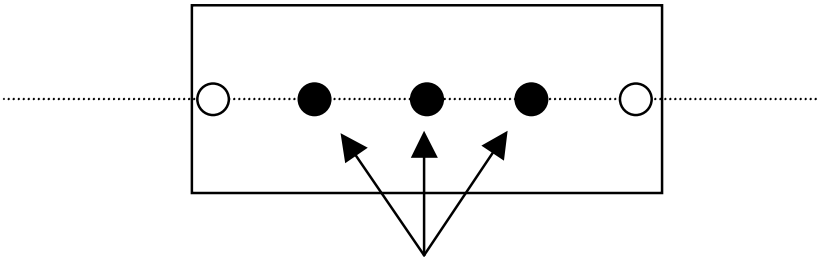
The mounting surface of the heat sink should be finished to a roughness of 10μm or less and a warp between screw holes of 100μm or less. If the surface of the heat sink is not flat enough, there will be a sharp increase in the contact thermal resistance (Rth(c-7)). If the flatness of the heat sink does not meet the above requirements, then attaching (clamping) an IGBT to it will place extreme stress on the DBC substrate situated between the module's chips and metal base, possibly destroying this insulating mateial.

3.3 Thermal compound application

To reduce contact thermal resistance, we recommend applying a thermal compound between the heat sink and the IGBT's base plate. When applying the thermal compound, either to the heat sink or the module's base, do so as shown in the diagram below. When the module is screwed down, the thermal compound will spread and force out any air, thereby ensuring an even contact. Possible thermal compounds are listed in **Table** 6-1.

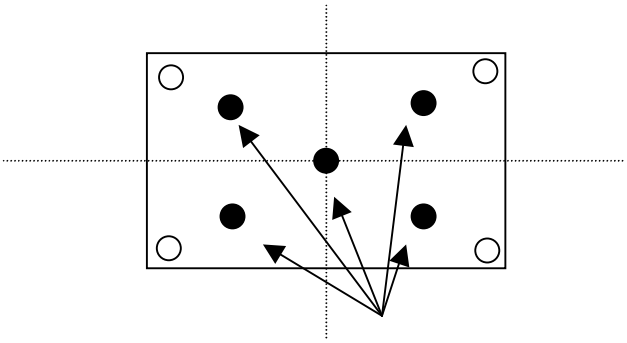
Table 6-1 Example of thermal compound

Product name	Manufacturer
G746	Shin-Etsu Chemical Co., Ltd.
SC102	Toray Dow-Corning Co., Ltd.
YG6260	Toshiba Silicone Co., Ltd.



Thermal compound (approx. 0.5g)

(1) Two-point module mounting



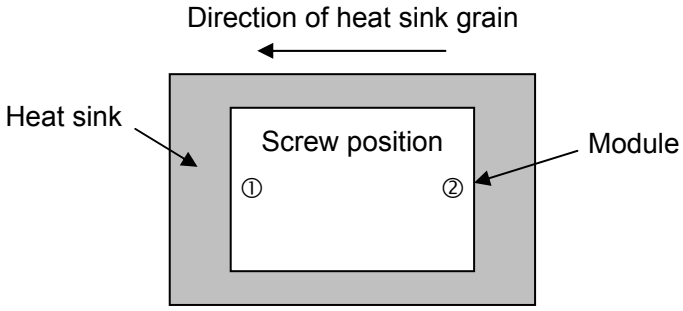
Thermal compound (approx. 0.5g)

(2) Four-point module mounting

Fig. 6-11 Thermal compound application

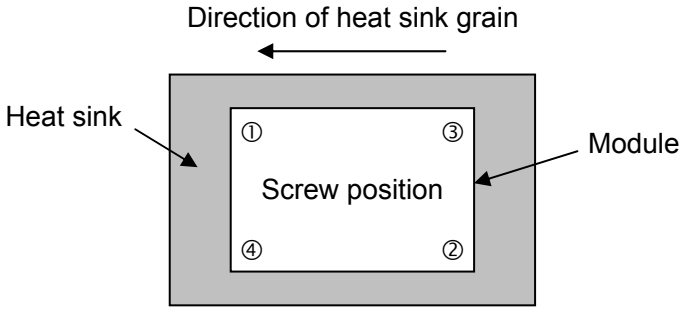
3.4 Mounting procedure

Figure 6-12 diagrams show how to tighten an IGBT module's mounting screws. Each screw must be tightened using a specified torque. For the proper tightening torque, refer to the module specification sheets. An insufficient tightening torque may cause the contact thermal resistance to increase or the screws to come loose during operation. On the other hand, an excessive tightening torque may damage the IGBT's case.



	Torque	Sequence
Initial	1/3 specified torque	①→②
Final	Full specified torque	②→①

(1) Two-point mounting



	Torque	Sequence
Initial	1/3 specified torque	①→②→③→④
Final	Full specified torque	④→③→②→①

(2) Four-point mounting

Fig. 6-12 IGBT module clamping

3.5 IGBT module mounting direction

When mounting the IGBT module, it is recommended to place the module lengthwise in the direction of the heat sink's grain. This reduces the effects of changes in the heat sink's shape.

3.6 Temperature verification

After deciding on a heat sink and mounting positions, measure the temperature of each area, and confirm that the junction temperature (T_j) of each module is within the required range.
For reference, Fig. 6-13 is a diagram of how to measure the case temperature (T_c).

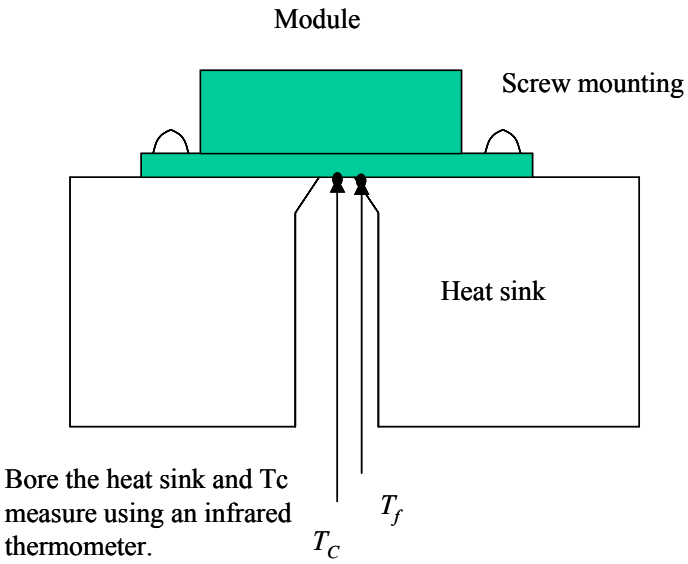


Fig. 6-13 Measurement of case temperature (Tc)

Chapter 7
Gate Drive circuit Design

CONTENTS **Page**

This section explains the drive circuit design.

In order to maximize the performance of an IGBT, it is important to properly set the drive circuit constants.

1 IGBT drive conditions and main characteristics

IGBT drive conditions and main characteristics are shown below. An IGBT's main characteristics change according to the values of VGE and RG, so it is important to use settings appropriate for the intended use of the equipment in which it will be installed.

Table 7-1 IGBT drive conditions and main characteristics.

Main characteristics	$+V_{GE}$ rise	$-V_{GE}$ rise	R_G rise
$V_{CE(sat)}$	Fall	-	-
t_{on} E_{on}	Fall	-	Rise
t_{off} E_{off}	-	Fall	Rise
Turn-on surge voltage	Rise	-	Fall
Turn-off surge voltage	-	Rise	Fall
dv/dt malfunction	Rise	Fall	Fall
Current limit value	Rise	-	Fall
Short circuit withstand capability	Fall	-	Rise *1
Radiational EMI noise	Rise	-	Fall

*: Non latch-up circuit is built into N series IGBT. Short circuit withstand capability depends on current limiting circuit characteristic.

1.1 $+V_{GE}$ (On state)

A recommended the gate on state voltage value (+ V_{GE}) is +15V. Notes when + V_{GE} is designed are shown as follows.

(1) Set $+V_{GE}$ so that is remains under the maximum rated G-E voltage, V_{GES} =±20V.
(2) It is recommended that supply voltage fluctuations are kept to within ±10%.
(3) The on-state C-E saturation voltage $V_{GE(sat)}$ is inversely dependent on $+V_{GE}$, so the greater the $+V_{GE}$ the smaller the $V_{GE(sat)}$.
(4) Turn-on switching time and switching loss grow smaller as $+V_{GE}$ rises.
(5) At turn-on (at FWD reverse recovery), the higher the $+V_{GE}$ the greater the likelihood of surge voltages in opposing arms.
(6) Even while the IGBT is in the off-state, there may be malfunctions caused by the dv/dt of the FWD's reverse recovery and a pulse collector current may cause unnecessary heat generation. This phenomenon is called a dv/dt shoot through and becomes more likely to occur as $+V_{GE}$ rises.
(7) In U series IGBTs, the higher the $+V_{GE}$, the higher the current limit becomes.
(8) The greater the $+V_{GE}$ the smaller the short circuit withstand capability.

1.2 $-V_{GE}$ (Off state)

A recommended the gate reverse bias voltage value ($-V_{GE}$) is –5 to -15V. Notes when $-V_{GE}$ is designed are shown as follows.

(1) Set $-V_{GE}$ so that it remains under the maximum rated G-E voltage, V_{GES} =±20V .
(2) It is recommended that supply voltage fluctuations are kept to within ±10%.
(3) IGBT turn-off characteristics are heavily dependent on $-V_{GE}$, especially when the collector current is just beginning to switch off. Consequently, the greater the $-V_{GE}$ the shorter, the switching time and the switching loss become smaller.

(4) If the $-V_{GE}$ is too small, dv/dt shoot through currents may occur, so at least set it to a value greater than –5V. If the gate wiring is long, then it is especially important to pay attention to this.

1.3 R_G (Gate resistance)

Listed in the product specification sheets under the heading of switching time using standard gate resistance. . Notes when R_G is designed are shown as follows.

(1) The switching characteristics of both turn-on and turn-off are dependent on the value of R_G, and therefore the greater the R_G the longer the longer the switching time and the greater the switching loss. Also, as R_G increases, the surge voltage during switching becomes smaller.
(2) The greater the R_G the more unlikely a dv/dt shoot through current becomes.
(3) N and S series IGBT modules have a built in overcurrent limiting capability and this overcurrent limit as well as the short circuit withstand capability are dependent on the value of R_G The greater the R_G the greater the short circuit withstand capability becomes, but conversely the current limit will drop. Therefore, it is important to set the overcurrent trip level of the equipment the modules will be installed in, to a value below this limit. At the recommended R_G value (Tj = 25°C), the lowest current limit point will be twice the rated current value.

Select the most suitable gate drive conditions while paying attention to the above points of interdependence.

2 Drive current

Since an IGBT has a MOS gate structure, to charge and discharge this gate when switching, it is necessary to make gate current (drive current) flow. Fig. 7-1 shows the gate charge (dynamic input) characteristics. These gate charge dynamic input characteristics show the electric load necessary to drive the IGBT and are used to calculate values like average drive voltage and the driving electric power. Fig. 7-2 shows the circuit schematic as well as the voltage and current waveforms. In principle, a drive circuit has a forward bias power supply alternately switching back and forth using switch S_1 and S_2. During this switching, the current used to charge and discharge the gate, is the driven current. In Fig. 7-2 the area showing the current waveform (the hatched area) is equivalent to the gate charge from Fig. 7-1.

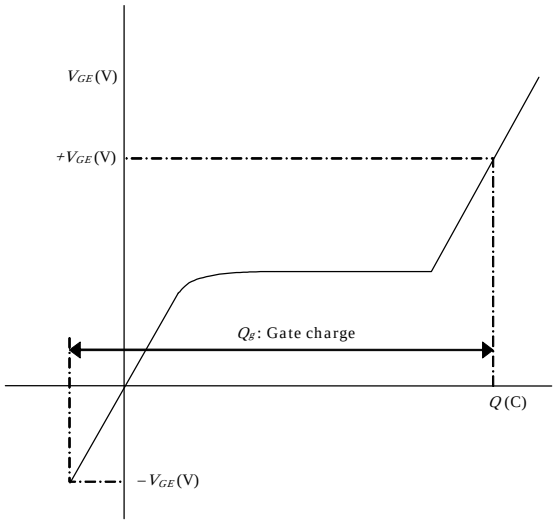


Fig. 7-1 Gate charge characteristics (Dynamic input characteristics).

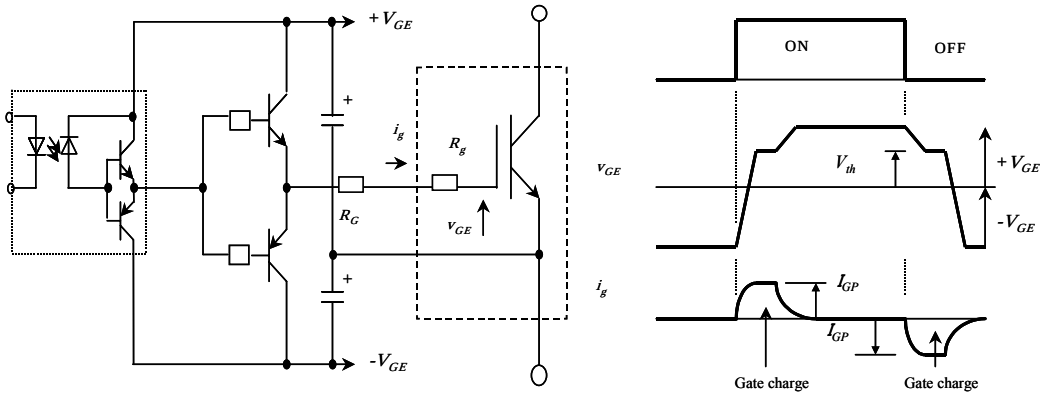


Fig. 7-2 Drive circuit schematic as well as voltage and current waveforms.

The drive current peak value I_{GP} can be approximately calculated as follows:

$$I_{GP} = \frac{+V_{GE} + |-V_{GE}|}{R_G + R_g}$$

$+V_{GE}$: Forward bias supply voltage
$-V_{GE}$: Reverse bias supply voltage
R_G : Drive circuit gate resistance
R_g : Module's internal resistance

Table 7-2 is shown in U series IGBT module internal gate resistance.

Table 7-2 U series IGBT module internal gate resistance.

Module withstand voltage (V)	Rated current (A)	Internal gate resistance (Ω)
600V	~ 200A	0 (None)
	300A, 400A	2.5
	600A	1.7
1200V	~ 50A	0 (None)
	75A ~ 150A	5
	150A ~ 300A (2 in 1)	2.5 (except 34 mm)
	300A (2 in 1)	2.5 (62 mm package) 1.7 (80 mm package)
	225A ~ 300A (6 in 1) A	1.7
	450A	1, 7
	600A, 800A	0.63

The slope of the gate charge characteristics (Refer to each modules technical specification sheets), rising from 0V is essentially the same as that of the input capacitance (Cies), and the reverse bias area can also be considered an extension of this. Therefore, the average value of the drive current IG, using the gate charge characteristics (Fig. 7-1), can be calculated as follows:

$$+I_G = -I_G = fc \times \left(Q_g + C_{ies} \times \left|-V_{GE}\right|\right)$$

fc : Carrier frequency
Q_g : Gate charge from 0V to $+V_{GE}$
C_{ies} : IGBT input capacitance

Consequently, it is important to set the output stage of the drive circuit in order to conduct this approximate current flow (IGB, as well as ±IG).
Furthermore, if the power dissipation loss of the drive circuit is completely consumed by the gate resistance, then the drive power (Pd) necessary to drive the IGBT is shown in the following formula:

$$Pd(on) = fc \bullet \left(\frac{1}{2} Q_g \left|+V_{GE}\right| + \frac{1}{2} C_{ies} \left|-V_{GE}\right|^2\right)$$

$$Pd(off) = Pd(on)$$

$$Pd = Pd(off) + Pd(on)$$

$$= fc \bullet \left(Q_g \left|+V_{GE}\right| + C_{ies} \left|-V_{GE}\right|^2\right)$$

Accordingly, a gate resistance is necessary that can charge this approximate capacity.
Be sure to design the drive circuit so that the above mentioned drive current and drive power can be properly supplied.

3 Setting dead-time

For inverter circuits and the like, it is necessary to set an on-off timing “delay” (dead time) in order to prevent short circuits. During the dead time, both the upper and lower arms are in the “off” state. Basically, the dead time (see Fig. 7-3) needs to be set longer than the IGBT switching time (toff max.). Accordingly, if RG is increased, switching time also becomes longer, so it would be necessary to lengthen dead time as well. Also, it is necessary to consider other drive conditions as well as the modules distribution and temperature characteristics, etc. (at high temperatures, toff becomes longer). It is important to be careful with dead times that are too short, because in the event of a short circuit in the upper or lower arms, the heat generated by the short circuit current may destroy the module.

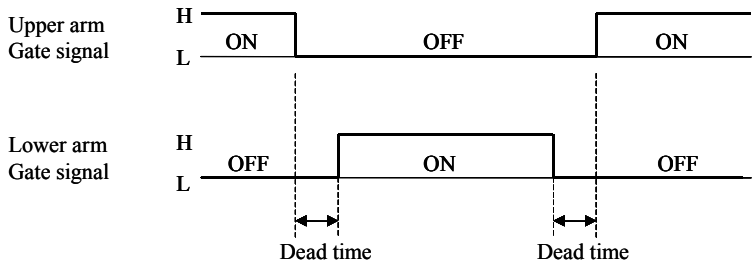


Fig. 7-3 Dead time timing chart.

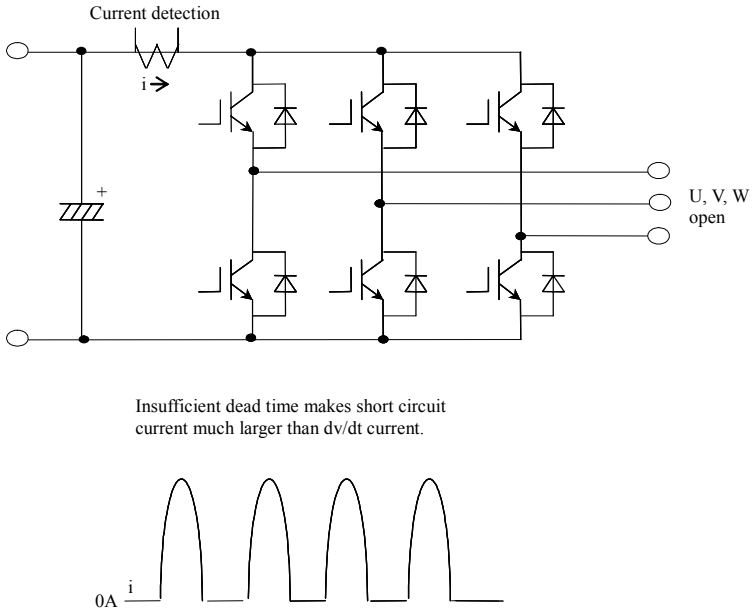


Fig. 7-4 Current detection methods for short circuit cased by insufficient dead time.

One method of judging whether or not the dead time setting is sufficient or not, is to check the current of a no-load DC supply line.
In the case of a 3-phase inverter (as shown in Fig. 7-4), set the inverter’s outputs to open, then apply a normal input signal, and finally measures the DC line current. A very small pulse current (dv/dt current leaving out the module’s Miller Capacitance: about 5% of the normal rated current) will be observed, even if the dead time is long enough.

However, if the date time is insufficient, then there will be a short circuit current flow much larger than this. In this case, keep increasing the dead time until the short circuit current disappears. Also, for the same reasons stated above, we recommend testing at high temperatures.

4 Concrete examples of drive circuits

For inverter circuits and the like, it is necessary to electrically isolate the IGBT from the control circuit. An example of a drive circuit using this principle, is shown below.
Fig. 7-5 shows an example of a drive circuit using a high speed opto-coupler. By using the opto-coupler, the input signal and the module are isolated from each other. Also, since the opto-coupler does not limit the output pulse width, it is suitable for changing pulse widths or PWM controllers, to wide ranges. It is currently the most widely used.
Furthermore, this way the turn-on and turn-off characteristics determined by gate resistance can be set separately, so it commonly used to ensure the best settings.
Fuji Electric is switching using opto-couplers to implement their Hybrid-ICs. (See Table below.)
Hybrid-ICs can drive with a single power supply, and also have a built in short circuit detection function as well as a soft cutoff circuit enabling them to provide the IGBT reliable protection in the event of a short circuit. For more complete details, refer to Hybrid-IC Application Manual. Aside from the above, there is also a signal isolation method using a pulse transformer. With this method the signal as well as the gate drive power can both be supplied simultaneously from the signal side, thereby allowing circuit simplification. However, this method has the limitations of an on/(off+on) time ratio of max. 50%, and reverse bias cannot be set, so its usefulness as a control method and switching frequency regulator is limited.

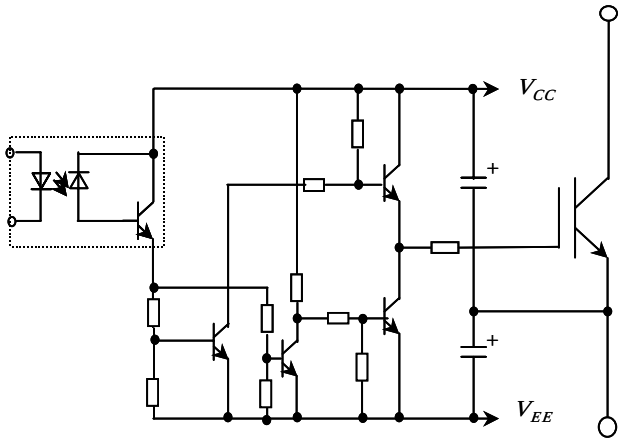


Fig. 7-5 Example of drive circuit using high speed opto-coupler.

Table 7-3 Hybrid ICs for driving IGBTs.

IGBT type / Suitable hybrid IC	600Vclass Up to 150A	600Vclass 200A to 400A
	1200Vclass Up to 75A	1200Vclass 100A to 300A
Medium speed type	EXB850	EXB851
High speed type	EXB840	EXB841

Medium speed type: Drive circuit signal transmission delay 4μs max.
High speed type: Drive circuit signal transmission delay 1.5μs max.

5 Drive circuit setting and actual implementation

5.1 Opto-coupler noise ruggedness

As IGBTs are high speed switching elements, it is necessary to select a opto-coupler for drive circuit that has a high noise ruggedness (e.g. HCPL4504). Also, to prevent malfunctions, make sure that the wiring from different sides doesn't cross. Furthermore, in order to make full use of the IGBT's a high speed switching capabilities, we recommend using a opto-coupler with a short signal transmission delay.

5.2 Wiring between drive circuit and IGBT

If the wiring between the drive circuit and the IGBT is long, the IGBT may malfunction due to gate signal oscillation or induced noise. A countermeasure for this is shown below in Fig. 7-6.

(1) Make the drive circuit wiring as short as possible and finely twist the gate and emitter wiring. (Twist wiring)
(2) Increase RG. However, pay attention to switching time and switching loss.
(3) Separate the gate wiring and IGBT control circuit wiring as much as possible, and set the layout so that they cross each other (in order to avoid mutual induction).
(4) Do not bundle together the gate wiring or other phases.

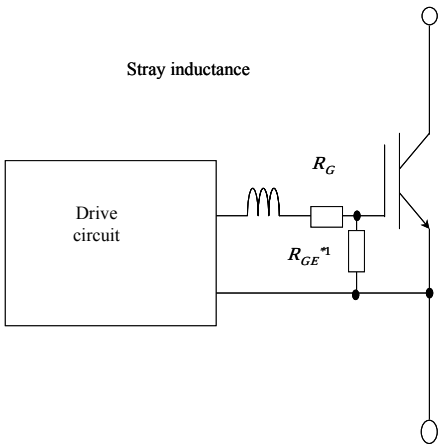


Fig. 7-6 Gate signal oscillation countermeasure

*1 R_{GE}
If the gate circuit is bad or if the gate circuit is not operating (gate in open state)*2 and a voltage is applied to the power circuit, the IGBT may be destroyed. In order to prevent this destruction, we recommend placing a 10kΩ resistance R_{GE} between the gate and emitter.
*2 Switch-on
When powering up, first switch on the gate circuit power supply and then when it is fully operational, switch on the main circuit power supply.

5.3 Gate overvoltage protection

It is necessary that IGBT modules, like other MOS based elements, are sufficiently protected against static electricity. Also, since the G-E absolute maximum rated voltage is ±20V, if there is a possibility that a voltage greater than this may be applied, then as a protective measure it is necessary to connect a zenner diode between the gate and emitter as shown in Fig. 7-7.

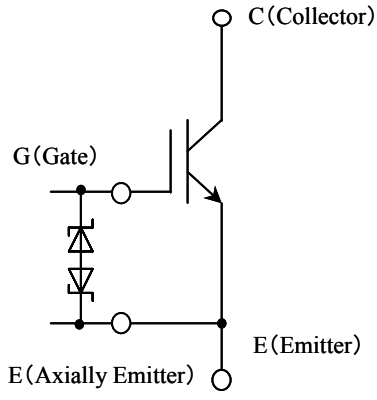


Fig. 7-7 G-E overvoltage protection circuit example.

Chapter 8
Parallel Connections

CONTENTS **Page**

This chapter explains the factors that inhibit current sharing and the notes when IGBT is connected in parallel.

When connecting IGBT modules in parallel, it is necessary to properly manage the elements' characteristics.
Otherwise, a current sharing imbalance may occur depend on the characteristics distribution between the parallel connected modules.

1 Factors that inhibit current sharing

1.1 On-state current imbalance

An on-state current imbalance may be caused by the following two factors:
(1) $V_{CE(sat)}$ distribution
(2) Main circuit wiring resistance distribution

1) Current imbalance caused by $V_{CE(sat)}$ distribution

As shown in Fig. 8-1, a difference in the output characteristics of two IGBT modules connected in parallel can cause a current imbalance.
The output characteristics of Q_1 and Q_2 shown in Fig. 8-1, can be approximated as follows:

$$V_{CEQ1} = V_{01} + r_1 \times I_{C1}$$

$$r_1 = V_1 / (I_{C1} - I_{C2})$$

$$V_{CEQ2} = V_{02} + r_2 \times I_{C2}$$

$$r_2 = V_2 / (I_{C1} - I_{C2})$$

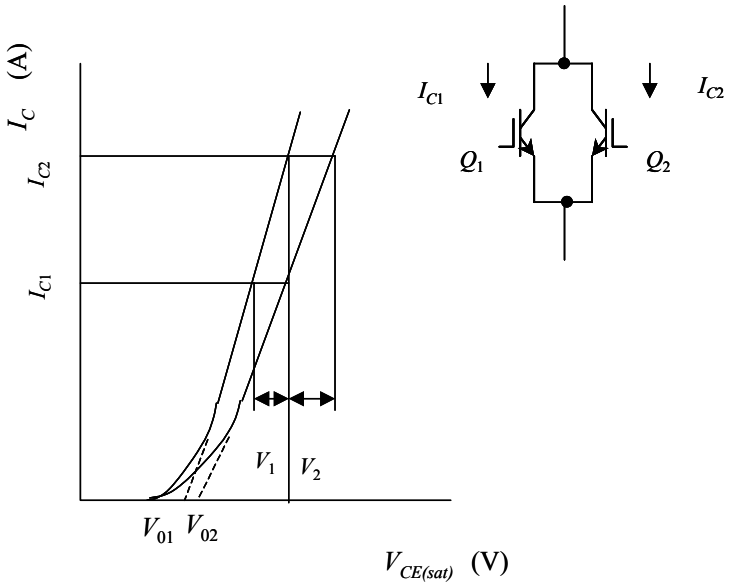


Fig. 8-1 Example of a $V_{CE(sat)}$ pair

Based on the above, if the I_{Ctotal} ($=I_{C1}+I_{C2}$) collector current is made to flow through the circuit of Q_1 and Q_2 connected in parallel, then the IGBT's collector current becomes the following:

$$I_{C1} = (V_{02} - V_{01} + r_2 \times I_{Ctotal}) / (r_1 + r_2)$$
$$I_{C2} = (V_{01} - V_{02} + r_1 \times I_{Ctotal}) / (r_1 + r_2)$$

$V_{CE(sat)}$ becomes a major factor in causing current imbalances. Therefore, in order to ensure the desired current sharing it is necessary to pair modules that have a similar $V_{CE(sat)}$.

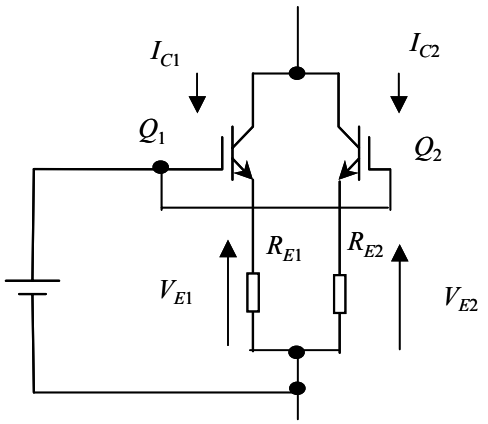


Fig. 8-2 The effect of main circuit wiring resistance

2) Main circuit wiring resistance distribution

The effect exerted on current sharing by the main circuit's wiring resistance can be seen in Fig. 8-2. The effect is larger with emitter resistance than with collector resistance, so collector resistance has been omitted here. If there is resistance in the main circuit, then the parity of the slope of the IGBT modules' output characteristics will lessen, and the collector current will drop. So, depending on how well the collector current can flow through this resistance, an electrical potential difference may appear,

the actual gate-emitter voltage drop (V_{GE}=V – VE), the IGBTs' output characteristics change and the collector current decline. Therefore, if $R_{E1}>R_{E2}$, then the slope of the Q_1 output characteristics will lessen and if $I_{C1}<I_{C2}$ then a current sharing imbalance will appear.
In order to reduce this imbalance, it is necessary to make the wiring on the emitter side as short and as uniform as possible.

1.2 Factors of current imbalances at turn-on and turn-off

The factors of current imbalances at turn-on and turn-off can be divided into module characteristics distribution and main circuit wiring inductance distribution.

1) Module Characteristics distribution

An IGBTs' switching current imbalance is mostly determined by an on-state current imbalance, therefore if the on-state current imbalance is controlled simultaneously, so will the switching voltage imbalance.

2) Main circuit wiring inductance distribution

Since the previously explained effect of resistance on current sharing is much the same as that of inductance on current sharing, inductance can be substituted for resistance in Fig. 8-2. As the collector current changes very suddenly during IGBT switching, a voltage is generated at both ends of inductance. The polarity of this voltage tends to hamper switching, so the switching time will increase. Therefore, if inductance is not controlled, then switching time will be delayed and the current will be concentrated into one of the modules. In order to reduce this imbalance, it is necessary to make the wiring on the emitter side as short and as uniform as possible.

2 Parallel connections

2.1 Wiring

The ideal parallel connection wiring is "both uniform and short", but when seen from the point of view of equipment mass production, it is often to implement this fully. Therefore, it is necessary to design a layout as close to the ideal as possible. For this purpose, several basic points of caution are illustrated below.

1) Drive circuit wiring

When connecting IGBT modules in parallel, due to the gate circuit's wiring inductance and the IGBT's input capacitance, as the gate voltage rises a parasitic oscillation may occur. Therefore, in order to prevent this oscillation, a gate resistor should be series wired to each of the modules gates. (As illustrated in Fig. 8-3)
As stated previously, if the drive circuit's emitter wiring is connected in a different position from the main circuit, then the modules' transient current sharing (especially at turn-on) will become imbalanced. However, IGBT modules have an auxiliary emitter terminal for use by drive circuits. By using this terminal, the drive wiring of each module becomes uniform, and transient current imbalances attribute to drive circuit wiring can be controlled.
Furthermore, be sure to lead the wiring out from the center of the modules parallel connection, tightly wind it together, and lay it out so that it is as far away from the main circuit as possible in order to avoid mutual induction.

2) Main circuit wiring

As stated previously, if the resistance or the inductance of the main circuit is not uniform, then the current sharing of the modules connected in parallel will be unbalanced.
Furthermore, if the inductance of the main circuit is large, then the surge voltage at IGBT turn-off will also be high (for details, refer to Chapter 5, “Protection Circuit Design”, of this manual). Therefore, for the purpose of reducing wiring induction and maintaining the temperature balance of each module, consider setting the modules that are to be connected in parallel as close together as possible and making the wiring as uniform as possible.
Also, take out the collector and emitter lead wires from the center of the parallel connection, and, in order to avoid mutual induction, do not wire them in parallel.

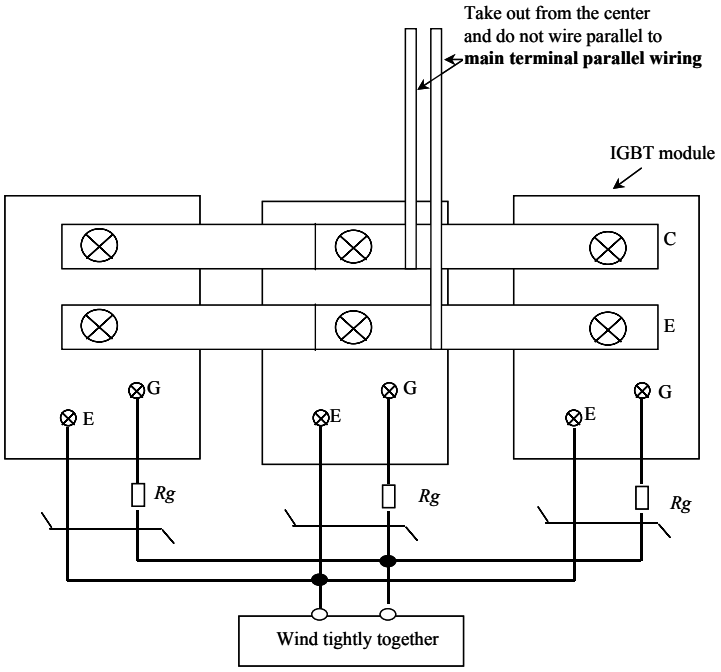


Fig. 8-3 Example of parallel connection layout

2.2 Relationship of module characteristics to current sharing

As stated previously, from among a module’s individual characteristics, the $V_{CE(sat)}$ distribution has a strong effect on current sharing.
When n-number of modules are connected in parallel, the following shows the maximum current that can be applied under the worst case conditions where the entire current is concentrated into one module:

$$\sum I = I_{C(\max)}\left[1+(n-1)\frac{\left(1-\frac{\alpha}{100}\right)}{\left(1+\frac{\alpha}{100}\right)}\right]$$

$$\alpha = \left[\frac{I_{C1}}{I_{C(ave)}} - 1\right] \times 100$$

Here $I_{C(max)}$ represents the maximum current for a single element that the modules rated RBSOA and power dissipation loss will allow. It is especially important to pay attention to power dissipation loss, because this changes depending on the operating conditions (switching frequency, drive conditions, heat dissipation, snubber conditions, etc.). For details on power dissipation loss, refer to Chapter 6, “Cooling Design”, of this manual. For example, if α=16%, $I_{C(max)}$=200A and n=4, then ΣI=634.4A, and the parallel connected total current should be set so as not to exceed this value. It is important not to make the error of simply calculatingΣI=200×4=800A.
Fig. 8-4 shows the difference of VCE(sat) and the current imbalance proportion in parallel connections. Because the temperature coefficient of the output characteristic is a positive characteristic as shown in Fig. 8-5, the current imbalance proportion α becomes small U-series IGBT compared with N-series IGBT.

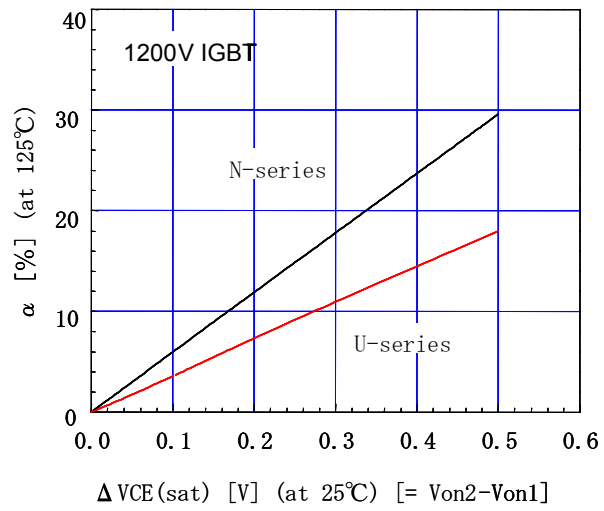


Fig. 8-4 Current imbalance proportion in parallel connections

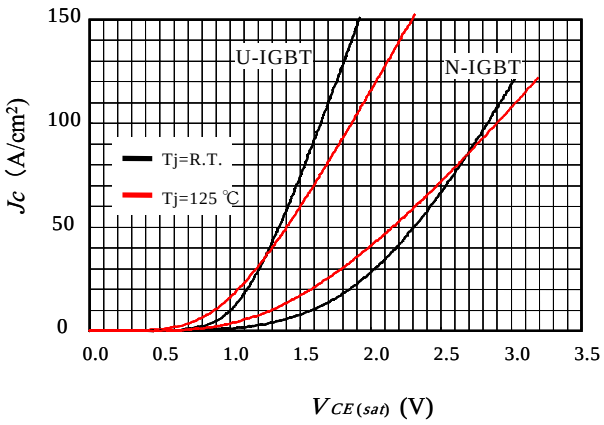


Fig. 8-5 Comparison of $V_{CE(sat)}$-Jc characteristics

Chapter 9
Evaluation and Measurement

CONTENTS Page

This section explains the method of evaluating the IGBT module characteristics and the measurement methods.

1 Application scope

This chapter provides instructions on how to evaluate the characteristics of IGBT modules used in power electronics having a switching frequency of several kHz to 100 kHz and an equipment capacitance of several hundred VA or more. It also provides instructions on how to measure IGBT module voltage and current.

2 Evaluation and measurement methods

2.1 Evaluation and measurement method summary

While power electronic test equipment is always under development, and it is necessary to evaluate the characteristics of a semiconductor device and measure its performance during its installation into circuits, use the correct equipment to capture this information.
Table 9-1 gives a summary description of the evaluation items and measurement methods.

Table 9-1 Evaluation item and measurement method summary.

No.	Evaluation item	Measured quantity	Measurement methods	Measuring equipment
1	Isolation voltage	Voltage	With the module terminals shorted, apply a voltage between the conductive part and the frame of the device.	Isolation voltage tester
2	Collector– Emitter voltage		With the Gate and Emitter shorted, apply test voltage to the Collector and Emitter. *If the applied test voltage exceeds the V rating of components connected to C & E, disconnect those components.	Curve tracer (Model 576, Sony Tektronix)
3	Collector-Emitter saturation voltage		Perform measurements with a voltage clamping circuit inserted between the Collector and Emitter to bypass the effect of the amplifier built in the oscilloscope. *Static characteristics can be measured with a curve tracer or pulse h_{FE} meter.	Oscilloscope
4	Surge voltage		Measure the voltage between the modules terminals directly for both the Collector and Emitter.	Oscilloscope
5	Switching time	Voltage Current	Measure the required voltage and current waveform according to the switching time definition.	Oscilloscope Current probe
6	Current sharing at parallel connection	Current	Measure the current through each device using current transformers for measurement.	Oscilloscope Current probe
7	Switching loss	Voltage Current	The product of the current and voltage is integrated during the switching time. (1) Calculate from the voltage and current waveforms. (2) Use a measuring instrument having math computing capability.	Oscilloscope (Model 7854, Model 2430A)
8	Operating locus		Plot the current and the voltage during switching action in current-voltage graph.	Oscilloscope with an X-Y display facility
9	Case temperature	Temperature	Measure on the copper base under the IGBT chip. *The case temperature measurement location is shown in chapter 3.	Thermocouple thermometer
10	Junction temperature		Have a calibration curve for the junction temperature and device characteristics created with regard to the temperature dependence of the device characteristics (for example, on resistance) and then measure the characteristics of the device in operation to estimate the junction temperature. *The method of measuring the junction temperature using the thermo-viewer directly.	Thermo-viewer

2.2 Voltage measurement

Voltage measurement relates to the measurement of such voltages as the transient voltage during switching action, the voltage in the brief on-state following switching action etc. Note that the accuracy of voltage measurement is affected by the noise interferences imparted from large-amplitude fast switching action.

(1) Measuring apparatus and calibration

Voltages are usually measured using an oscilloscope for the measuring apparatus, because their waveform, as well as the measurement value, is important. Voltage probes are used for voltage measurement.
The time constants of the voltage divider RC of the probe and oscilloscope vary depending on the oscilloscope-probe combination. Before using the probe, carry out probe compensation to achieve uniform attenuation across the frequency range by using the calibrator output and voltage of the oscilloscope.
With an appropriate sensitivity setting (generally, 3 to 4 div amplitude on the display screen), set the input coupling to DC. Exercise caution in selecting the probe, because the adjustment capacitance of the probe and the input capacitance of the oscilloscope must match to enable adjustment.
The selection of oscilloscopes and probes are shown in sections 9-5 and 9-6.

(2) Saturation voltage measurement

Generally, while the circuit voltage under which an IGBT is used comes as high as several hundred Volts, the saturation voltage is as low as several Volts. Because the size of the CRT screen used in an oscilloscope is generally finite, raising the voltage sensitivity in an effort to read the saturation voltage accurately will result in the display of a waveform that is different from the actual waveform, primarily because of the effect of the saturation of the oscilloscope's internal amplifier.
Accordingly, the IGBT saturation voltage during the switching action cannot be known by directly measuring the voltage between the device collector and emitter. Therefore, measure the saturation voltage by adding a voltage clamping circuit shown in Fig. 9-1.

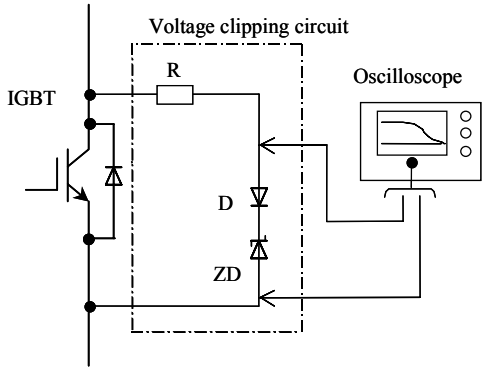


Fig. 9-1 Saturation voltage measurement method

In Fig. 9-1, the Zener diode (ZD) limits the high voltage when the IGBT is turned-off. Generally, a Zener diode of 10V or less is used. R denotes a current-limiting resistance. Because a large proportion of the circuit voltage is applied to this resistance when the IGBT is turned-off, the resistance must have a relatively large value. The diode (D) prevents the charges built in the junction capacitance of the Zener diode (ZD) from discharging, and also prevents a filter from being formed of the junction capacitance and the current-limiting resistance.

(3) Surge voltage measurement (Collector – emitter voltage measurement)

While IGBTs offer the benefit of fast switching, they have a high ratio of turn-off current change (-di/dt), inducing a high voltage in the main circuit wiring inductance (ls) of the equipment. This voltage is superimposed over the DC circuit voltage to creating a spike voltage to the module. It is necessary to verify that this voltage has a predefined voltage margin, established by the designer, with respect to the maximum voltage ratings.
The surge voltage can be measured at the terminals of the module with an oscilloscope and then directly reading the value on the CRT screen. When making these measurements, keep the following precautions in mind:

(I) Use a probe and an oscilloscope having a sufficient frequency bandwidth.
(II) Adjust the oscilloscope sensitivity and calibrate the probe.
(III) Connect the measurement probe directly to the module terminals.

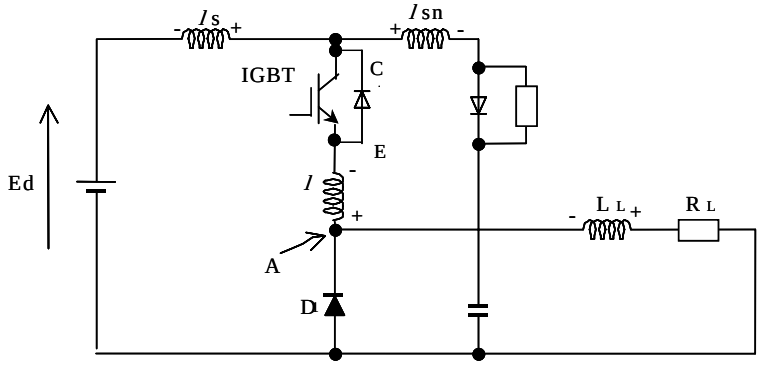


Fig. 9-2 Surge voltage measurement circuit

A voltage of the polarity shown in Fig. 9-2 is induced in the circuit inductances during turn-off. Note that in cases where V_{CA} instead of V_{CE}, is measured at this point as an initial voltage, then a voltage lower than VCE by –l*di/dt will be erroneously measured.

(IV) Keep the probe measurement leads as short as possible.
(V) Keep probe leads away from high di/dt areas so that noise interferences are not picked up.

If the voltage probe is connected to the circuit under the IGBT, the reference potential of the oscilloscope would equal the switching circuit. If there is a large ground potential variation in the switching circuit, common-mode current would flow through the power line of the oscilloscope, causing its internal circuit to malfunction. Noise interferences can be verified, for example, by:
(I) Debating whether the standing wave can be logically explained.
(II) Comparing with wave forms observed on a battery-powered oscilloscope that is less susceptible to noise interferences.

(4) Gate voltage measurement (Gate-emitter voltage measurement)

Although the gate-emitter voltage, like the initial voltage, can be directly measured on an oscilloscope, care should be taken to prevent noise interferences during probe connection and disconnection. This is largely due to the high impedance of the signal source and the gate resistance connected in series with the gate of the IGBT.
The measurement deserves similar attention as in the initial voltage measurement.

2.3 Current measurement

Current probes are used for current measurement. Because practical devices have their main circuitry downsized to cut wiring inductances and simplify their geometry, the wiring needs to be extended to measure the device current. A current transformer can be used to minimize the wiring extension and thus to cut its effect as much as possible. The use of current transformers is also necessary to make up for the limited measuring capacity of the current probe.
A current probe maintains insulation from the conductive part to enable current measurement, but, in addition to being an electromagnetic induction-based detector, it has such a low signal level that it is susceptible to induction-caused noise interferences. Care should be taken, therefore, to guard against noise interferences.

(1) Current detectors

Table 9-2 lists examples of the current detectors.

Table 9-2 Current detectors

No.	Description	Model	Brand	Remarks
1	DC current probe Dedicated amplifier and power supply required	Model A6302	Sony Tektronix	Maximum circuit voltage: 500V Up to 20 A at DC to 50 MHz Up to a peak pulse current of 50A
2		Model A6303		Maximum circuit voltage: 700V Up to 100A at DC to 15MHz Up to a peak pulse current of 500 A
3	AC current probe	Model P6021		Maximum circuit voltage: 600V Up to 15Ap-p at 120Hz to 60MHz, Peak pulse current: 250A
4		Model P6022		Maximum circuit voltage: 600V Up to 6Ap-p at 935Hz to120MHz Peak pulse current: 100A
5	ACCT	Varied	Pearson	Less than 35MHz

(2) Current probe sensitivity check

Before making any measurements, it is necessary to check the probe sensitivity. Use the calibrator output of the oscilloscope or use an oscillator to calibrate the current probe shown in Fig. 9-3.
The measurement method of Fig. 9-3 uses resistance R (No induced drag is used). Both voltage (e) and R is measured. This voltage (e) is divided by R and current (i) is obtained. These currents are compared with the shape of waves of the current probe and checked for accuracy. If the current (i) is too small, increase primary winding of the current probe.

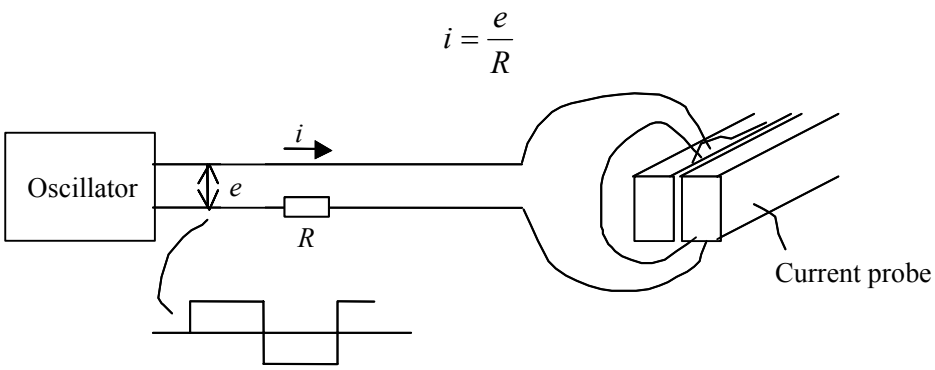


Fig. 9-3 Current probe calibration method

(3) Current measurement method

Fig. 9-4 shows where current transformers (CT) are inserted to measure the current through a semiconductor device, and the method of current measurement with two devices connected in parallel.

When the current of T11 on the part of a positive arm is measured, the second side current of CT1 is measured with the current probe. Moreover, the current of T12 measures the side current of the second ditto CT2 with the current probe. The current of the positive side arm (total of the current of the current of T11 and T12) can be measured with the same current probe by measuring in bulk after the direction of the second side current of CT_1 and CT_2 is matched. Please refer to sections 9-6 and 9-7 for the application of the current probe and transducers.

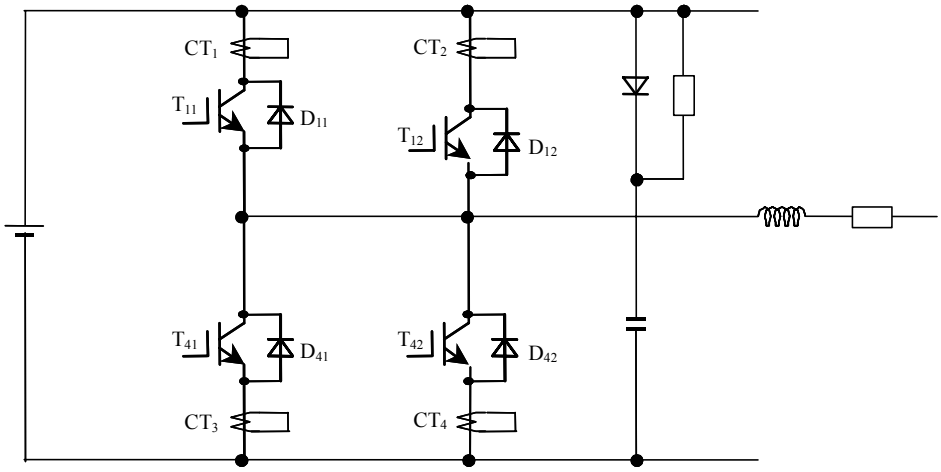


Fig. 9-4 Current measurement method

2.4 Switching loss measurement

The switching loss must be the loss generated between the two instants of time at which switching starts and at which the effect of switching is lost. The turn-on loss, for example, is the loss that is generated after the gate and source are forward-biased until the drain-source voltage reaches the saturation voltage. The switching loss is generally expressed in terms of the energy generated per instance of switching.

Fig. 9-5 shows examples of switching waveforms and switching losses. Correct current and voltage waveform measurement is prerequisite to switching loss measurement. Note that when current and voltage are measured simultaneously, the common-mode current flowing from the voltage probe causes the current waveform to be distorted. The presence or absence of a common-mode effect

can be determined by comparing the current waveforms associated with the availability and non-availability of voltage probes. If the current waveform is distorted, insert common-mode chokes (cores with excellent high frequency characteristics having a cable wound on them) into the voltage probe and oscilloscope power cables as shown in Fig. 9-6 to alleviate the distortion.
Equally important is the settings of reference 0V and 0A. Note that, in current measurement operations using an AC current probe, the position of 0A varies depending on the measurement current value and the conduction ratio.
Apparatus with a waveform computing facility that are capable of switching loss measurement with relatively good accuracy include:
Processing oscilloscope Model 7854 (Sony Tektronix)
Digital memory scope Model 2430A (Sony Tektronix)

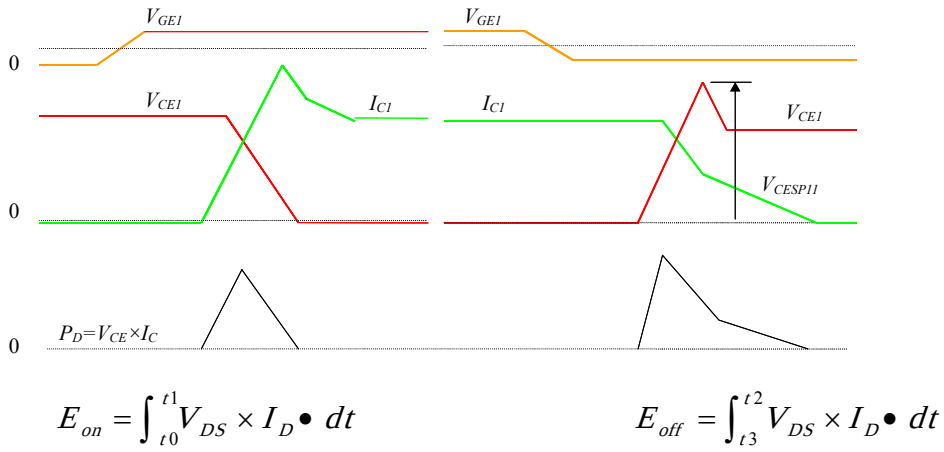


Fig. 9-5 Switching losses

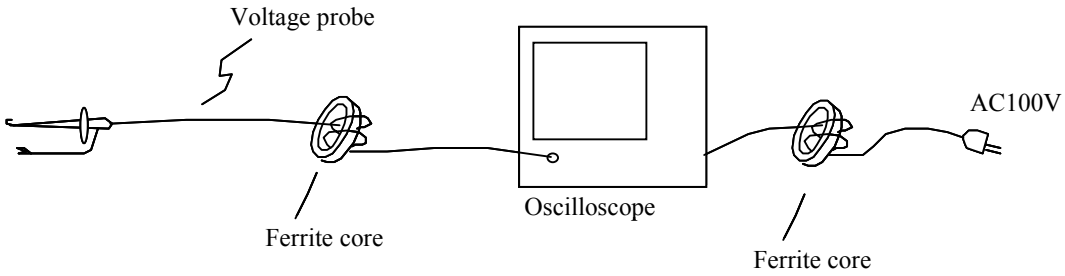


Fig. 9-6 Inserting common mode chokes

2.5 Selecting oscilloscopes

Because oscilloscopes vary in terms of functionality and performance, it is important to select the right oscilloscope to suit the measurement items required and the rate of change in the signal of interest. This section provides a summary description of the signal source rise time and the frequency bandwidth requirements for the oscilloscopes to be used.

(1) Relationship between the rise time of a pulse waveform and the frequency band

The rise time of a pulse waveform is defined as the time needed for the voltage to vary from 10% to 90% as shown in Fig. 9-7.

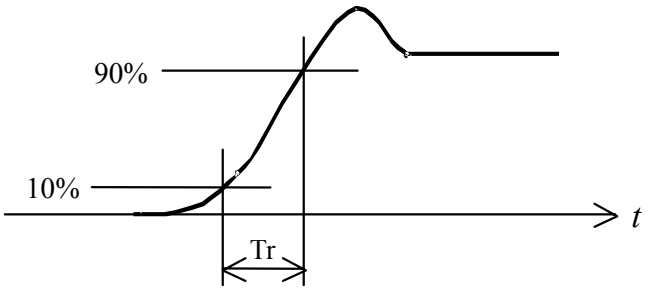


Fig. 9-7 Definition of the rise time of a pulse waveform

Assuming that the rise time is Tr and the frequency at which -3 dB is attained is F_{-3dB}, then the following relationship holds between them:

$$T_r \times F_{-3dB} \fallingdotseq 0.35 \quad \cdots\cdots (1)$$

(2) Signal source rise time (T_{r1}) and oscilloscope selection

Fig. 9-8 shows the rise time of each component of an actual system of measurement.

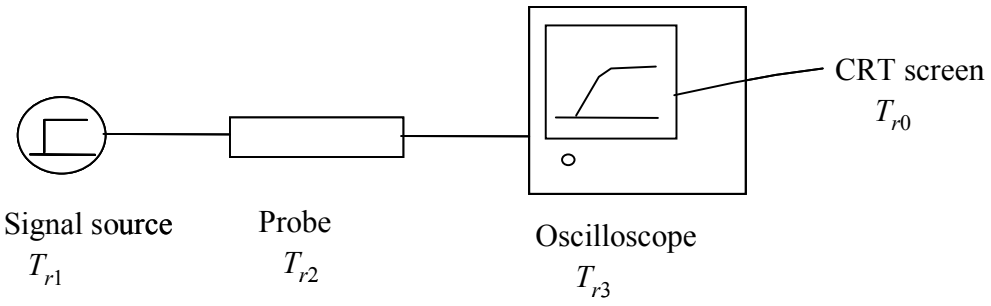


Fig. 9-8 System of measurement and component rise time

The rise time T_{r0} of the waveform displayed on the CRT screen of the oscilloscope is determined by the component rise time and is expressed as:

$$T_{r0} = \sqrt{{T_{r1}}^2 + {T_{r2}}^2 + {T_{r3}}^2} \quad \cdots\cdots (2)$$

A correct reproduction of the waveform of the signal source is accomplished by setting $T_{r0} = T_{r1}$. Assuming that:

$$\varepsilon = \frac{T_{r0} - T_{r1}}{T_{r1}} \times 100 \ \ (\%), \ \ k = \frac{T_{r2} + T_{r3}}{T_{r1}} \quad \cdots\cdots (3)$$

If Eq.(2) is used to determine the relationship between ε and k, it would be as tabulated in Table 9-3.

Table 9-3 Waveform measurement errors, and signal source and measuring apparatus startup time ratios

ε (%)	1	2	3
K	7	5	4

According to these relationships, the sum total of the probe and oscilloscope startup times must not exceed one fourth of the rise time of the signal source. (Exp. Tr0 = 3.5ns, ε = 3%, 3.5/4 = 0.87 ns)
If the startup time of the probe is disregarded, solving Eq. (1) gives the required frequency band of the

oscilloscope as $0.35/0.87 \times 10^{-9} = 4 \times 10^{8}$, or 400 MHz. Accordingly, an oscilloscope having a frequency band of 400 MHz or above must be used.
Thus, the selection of the oscilloscope to be used should reflect the rise time of the signal of interest.

2.6 Selecting probes

Probes are available in two types as mentioned earlier: voltage probes and current probes.
This section provides basic hints on selecting probes and their usage tips.

2.6.1 Voltage probes

(1) Rise time

It is important to allow for a frequency band for the probe to be used that is in accordance with the rise time of the signal of interest as explained in 9.7. The concept of probe selection is similar to the concept of oscilloscope selection and is not defined here.

(2) Effects of the signal source impedance and probe capacitance on the rise time

An electrical equivalent circuit of the system of measurement is shown in Fig. 9-9, in which R_1 and C_1 denote the output impedance and capacitance of the signal source, respectively, and R_2 and C_2 denote the input impedance and capacitance of the oscilloscope, respectively.

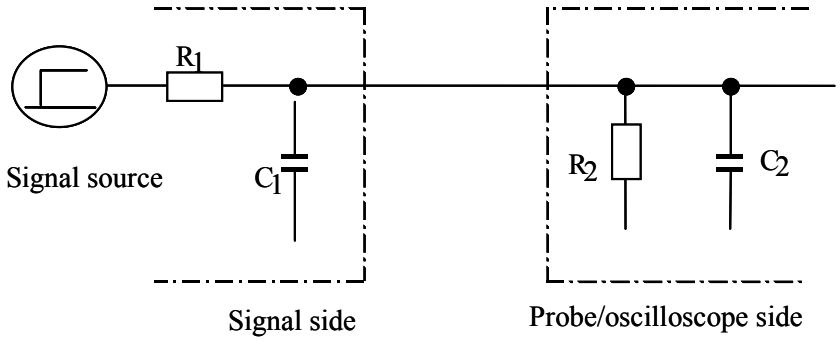


Fig. 9-9 Electrical equivalent circuit of the system of measurement

The rise time *Tr* of the C-R filter can be expressed by:

$$T_r = 2.2 \times R \times C$$

In Fig. 9-9, R and C can be expressed in equations as:

$$R = \frac{R_1 \times R_2}{R_1 + R_2} \qquad C = C_1 + C_2$$

The following facts become apparent from these relationships:

1) The higher the output impedance of the signal source, the longer the rise time becomes.
2) This also holds true with probes or oscilloscopes having a large capacitance:

   ① For example, if the signal of a signal source (R1 = 500Ω, C1 = 2 pF) is measured using an ordinary passive 10:1 probe (C2 = 9.5 pF, R2 = 10 MΩ), a rise time of 12ns, would result from the connection of the probe, compared with 2.2 ns without its connection, generating a significant error.

(3) Probe selection

Table 9-4 summarizes the conditions for selecting probes to suit specific measurement objectives and tips on measurement using these probes.

Table 9-4 Conditions for selecting probes to suit specific objectives of measurement

Measurement / Item	Amplitude measurement	Rise time	Phase difference
Probe requirements	The input impedance must be high in the working frequency band.	A sufficient frequency band is available for the rise time of the signal source.	Low input capacitance Matched cable lengths and characteristics
Directions	The pulse width is at least five times the time constant of the probes and the oscilloscope. Select a signal source of the lowest impedance possible.	The pulse width is at least five times the time constant of the probes and the oscilloscope. Select a signal source of the lowest impedance possible.	Measure the probe-to-probe time difference beforehand. *A 3.5-feet probe has a delay of 5 ns.

(4) Directions

Correct signal measurement requires an understanding of the characteristics of probes to make a correct choice. Key items to consider when selecting a probe are listed below.

a. Does the probe have the current range to measure the desired target voltage/current.
b. Is the frequency bandwidth of the probe correct for the measurement?
c. Is the maximum input (withstand voltage) adequate?
d. Will the loading effect of the probe cause a false reading? (optimal measuring points)
e. Is the ground (earth wire) connected properly?
f. Are there mechanical or physical strains?

In measuring fast switching pulses, grounding should be checked carefully. In this case, resonance could arise from the inductance of the ground lead and the probe capacitance. Such resonance would be particularly pronounced in a broadband oscilloscope. Shortening the probe ground lead to ground and the tip can reduce resonance or oscillation. An adapter usually comes with each voltage probe as an accessory for this purpose.
In addition, a ground lead may be connected to each individual probe to guard against induction-caused noise interferences shown in Fig. 9-10. The points to which the ground leads are connected must have equal potentials in this case.

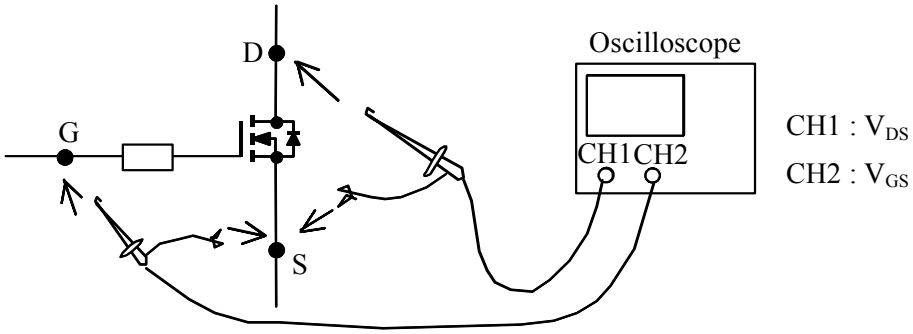


Fig. 9-10 Connecting voltage probes

2.6.2 Current probes

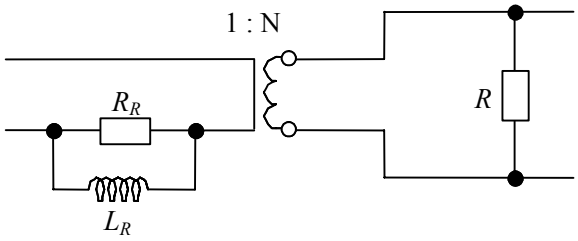
The types of current probes available are as described in 2.3. This section focuses on tips on using current probes in actual applications.

(1) Current probe selection

Current probes are available in two types as mentioned earlier: DC current probes and AC current probes. AC current probes, with their better noise immunity, are recommended for use in measuring current waveforms during fast switching action.
If a DC or low-frequency AC current is introduced through an AC current probe, the core in the probe would be saturated to suppress output. To measure the switching action of an IGBT used in a circuit that deals with a DC or low-frequency AC, some techniques are necessary, such as fabricating and using a timing control circuit to simulate the actual action.

(2) Use precautions

a. A ferrite core is housed in the tip of a current probe. The ferrite core is extremely vulnerable to impact and must be protected against dropping.
b. Be careful not to exceed the ratings.
   - Withstand voltage: If the circuit voltage is high, cover the measuring point with a voltage-resistant tube.
   - A-S (current product): Pulse current rating. Excessive current flow could cause damage to the probe.
   - Maximum RMS current immunity: Limited by the power capacitance of the secondary circuit in the probe transformer. The probe could be burned if this limit is exceeded.
c. With a voltage clamping circuit, perform measurement with the current probe being securely clipped to the circuit.
d. Do not release the secondary side of the circuit with the current probe clipped to the circuit. (Without a terminator in position, a high voltage could be generated on the secondary side.)
e. Insertion impedance
   Inserting the probe into position generates an insertion impedance on the primary side of the circuit. It is important to ensure that the insertion impedance does not affect the measuring object.
   Assuming that the probe is an ideal transformer, the insertion impedance can be expressed in Fig. 9-11.



$$L_R = \frac{\text{Secondary inductance } (L)}{N^2}$$

$$R_R = \frac{\text{Secondary load resistance } (R)}{N^2}$$

Fig. 9-11 Probe insertion impedance

2.7 Using current transformers

A current transformer is used to ease the constraint on the working range of a current probe and to minimize the effects partial modifications made to measurement purposes may have upon circuit performance. For information on the locations where current transformers are inserted and instructions on how to measure current, see Fig. 9.3.

Assuming that the number of turns (secondary) of the transformer is N, and the primary current is I_1 and the secondary current is I_2, an ideal transformer would meet the relationship $I_2 = I_1/N$. With the excitation current taken into account, the relationship can be rewritten as:

$$I_O = I_1 - N \times I_2$$

The excitation current must be a small value because it creates a measurement error. Check the value of N with regard to the transformer, measure I_1 and I_2 and calculate I_0 from the equation above to make sure that the measurement accuracy is acceptable.
Next, check the direction of the current flow. Current flows through the secondary winding in such direction that a magnetic flux generated in the core by the primary current is canceled.
Be careful not to drop the ferrite core because it could be damaged.

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   The contents are subject to change without notice for specification changes or other reasons. When using a product listed in this Catalog, be sure to obtain the latest specifications.

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